VT1432B

4-/8-/16-CHANNEL, 102.4 kSa/s DIGITIZER PLUS DSP

VT1435

4-/8-CHANNEL, 102.4 kSa/s DIGITIZER PLUS DSP
WITH IEPE CURRENT SOURCE AND TEDS SUPPORT

VT1436

16-CHANNEL, 102.4 kSa/s DIGITIZER PLUS DSP
WITH IEPE CURRENT SOURCE AND TEDS SUPPORT

USER'S MANUAL

P/N: 82-0110-000
Released July 20, 2010

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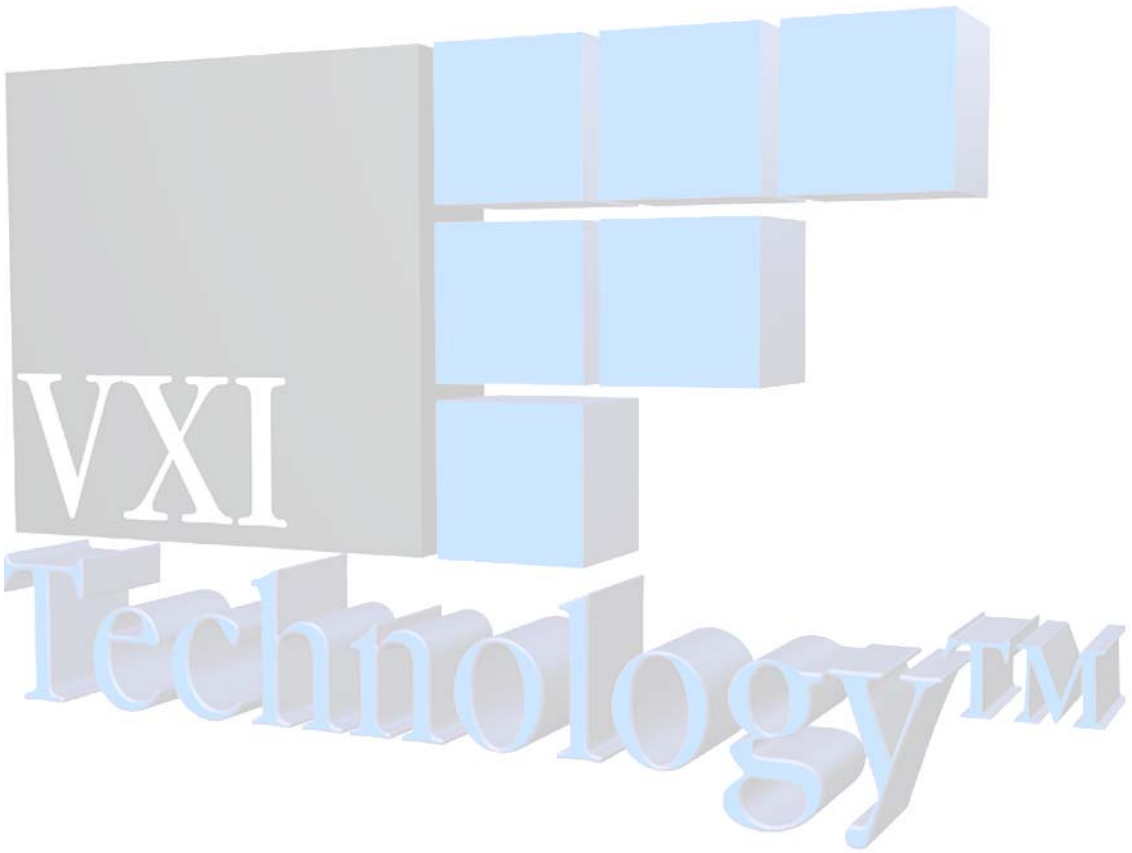
VXI
Technology™

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CERTIFICATION

VXI Technology, Inc. (VTI) certifies that this product met its published specifications at the time of shipment from the factory. VTI further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

The product referred to herein is warranted against defects in material and workmanship for a period of three years from the receipt date of the product at customer's facility. The sole and exclusive remedy for breach of any warranty concerning these goods shall be repair or replacement of defective parts, or a refund of the purchase price, to be determined at the option of VTI.

For warranty service or repair, this product must be returned to a VXI Technology authorized service center. The product shall be shipped prepaid to VTI and VTI shall prepay all returns of the product to the buyer. However, the buyer shall pay all shipping charges, duties, and taxes for products returned to VTI from another country.

VTI warrants that its software and firmware designated by VTI for use with a product will execute its programming when properly installed on that product. VTI does not however warrant that the operation of the product, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The warranty shall not apply to defects resulting from improper or inadequate maintenance by the buyer, buyer-supplied products or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

VXI Technology, Inc. shall not be liable for injury to property other than the goods themselves. Other than the limited warranty stated above, VXI Technology, Inc. makes no other warranties, express or implied, with respect to the quality of product beyond the description of the goods on the face of the contract. VTI specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

RESTRICTED RIGHTS LEGEND

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subdivision (b)(3)(ii) of the Rights in Technical Data and Computer Software clause in DFARS 252.227-7013.

VXI Technology, Inc.
2031 Main Street
Irvine, CA 92614-6509 U.S.A.

DECLARATION OF CONFORMITY

Declaration of Conformity According to ISO/IEC Guide 22 and EN 45014

MANUFACTURER'S NAME	VXI Technology, Inc.
MANUFACTURER'S ADDRESS	2031 Main Street Irvine, California 92614-6509-6509
PRODUCT NAME	4-/8-/16-channel, 102.4 kSa/s Digitizer with DSP
MODEL NUMBER(S)	VT1432B, VT1435, VT1436
PRODUCT OPTIONS	All
PRODUCT CONFIGURATIONS	All

VXI Technology, Inc. declares that the aforementioned product conforms to the requirements of the Low Voltage Directive 73/23/EEC *and the* EMC Directive 89/366/EEC *(inclusive* 93/68/EEC*) and carries the "CE" mark accordingly. The product has been designed and manufactured according to the following specifications:*

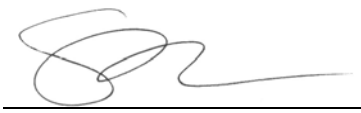
SAFETY	EN61010 (2001)
EMC	EN61326 (1997 w/A1:98) Class A CISPR 22 (1997) Class A VCCI (April 2000) Class A ICES-003 Class A (ANSI C63.4 1992) AS/NZS 3548 (w/A1 & A2:97) Class A FCC Part 15 Subpart B Class A EN 61010-1:2001

The product was installed into a C-size VXI mainframe chassis and tested in a typical configuration.

I hereby declare that the aforementioned product has been designed to be in compliance with the relevant sections of the specifications listed above as well as complying with all essential requirements of the Low Voltage Directive.

June 2007

CE



Steve Mauga, QA Manager

GENERAL SAFETY INSTRUCTIONS

Review the following safety precautions to avoid bodily injury and/or damage to the product. These precautions must be observed during all phases of operation or service of this product. Failure to comply with these precautions, or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture, and intended use of the product.

Service should only be performed by qualified personnel.

TERMS AND SYMBOLS

These terms may appear in this manual:

WARNING Indicates that a procedure or condition may cause bodily injury or death.

CAUTION Indicates that a procedure or condition could possibly cause damage to equipment or loss of data.

These symbols may appear on the product:

ATTENTION - Important safety instructions

Frame or chassis ground

Indicates that the product was manufactured after August 13, 2005. This mark is placed in accordance with *EN 50419, Marking of electrical and electronic equipment in accordance with Article 11(2) of Directive 2002/96/EC (WEEE)*. End-of-life product can be returned to VTI by obtaining an RMA number. Fees for take-back and recycling will apply if not prohibited by national law.

WARNINGS

Follow these precautions to avoid injury or damage to the product:

Use Proper Power Cord To avoid hazard, only use the power cord specified for this product.

Use Proper Power Source To avoid electrical overload, electric shock, or fire hazard, do not use a power source that applies other than the specified voltage.

Use Proper Fuse To avoid fire hazard, only use the type and rating fuse specified for this product.

WARNINGS (CONT.)

Avoid Electric Shock

To avoid electric shock or fire hazard, do not operate this product with the covers removed. Do not connect or disconnect any cable, probes, test leads, etc. while they are connected to a voltage source. Remove all power and unplug unit before performing any service. ***Service should only be performed by qualified personnel.***

Ground the Product

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground.

Operating Conditions

To avoid injury, electric shock or fire hazard:

- Do not operate in wet or damp conditions.
- Do not operate in an explosive atmosphere.
- Operate or store only in specified temperature range.
- Provide proper clearance for product ventilation to prevent overheating.
- DO NOT operate if any damage to this product is suspected. ***Product should be inspected or serviced only by qualified personnel.***

Improper Use

The operator of this instrument is advised that if the equipment is used in a manner not specified in this manual, the protection provided by the equipment may be impaired. Conformity is checked by inspection.

SUPPORT RESOURCES

Support resources for this product are available on the Internet and at VXI Technology customer support centers.

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Visit *http://www.vxitech.com* for worldwide support sites and service plan information.

SECTION 1

INSTALLING THE VT1432B

OVERVIEW

VXI Technology's VT1432B, VT1435, and VT1436 digitizers (henceforth referred to as "VT1432B", except where differences exist) are C-size, single slot, register-based VXI modules that include digital signal processing (DSP), transducer signal conditioning, alias protection, digitization, and high-speed measurement computation. In addition to these features, the VT1435 and VT1436 modules have integrated electronics piezoelectric (IEPE) current sources as well as optional transducer electronic data sheet (TEDS) support.

An optional arbitrary source or dual-input tachometer can be added to the VT1432B, for increased measurement functionality. On-board computation of measurement results, fast data transfer to the host computer, and a dedicated high-speed data bus for module-to-module communication all combine to provide outstanding measurement architecture for demanding mechanical, acoustic, and electrical test applications.

Putting so much capability into these instruments decreases system cost while increasing system performance. The VT1432B may contain up to four 4-channel input assemblies, giving them up to 16 inputs channels. On-board DSP and 32 MB of RAM maximize total system performance and flexibility. The new, redesigned 24-bit digitizer input combined with a large number of input ranges allow the VT1432B to operate in the most optimum measurement range. Even low sensitivity/low output level transducers work well with the VT1432B. The high performance floating point DSP used for the linear phase FIR anti-alias filters is also user programmable with TI's Code Composer Studio™. A standard JTAG interface is included to ease interfacing to this DSP. The FIR anti-alias filter vastly improves the phase accuracy of all channels relative to the tachometer, trigger, and other channels.

INSPECTING THE VT1432B

The VT1432B module was carefully inspected both mechanically and electrically before shipment. They should be free of marks or scratches and they should meet their published specifications upon receipt.

If the module was damaged in transit, do the following:

- Save all packing materials.
- File a claim with the carrier.
- Call a VXI Technology sales and service office.

INSTALLING THE VT1432B

CAUTION	To protect circuits from static discharge, observe anti-static techniques whenever handling a VT1432B module.

1. Set up the VXI mainframe. See the mainframe's installation guide for assistance.
2. Select a slot in the VXI mainframe for the VT1432B module. The module's local bus receives ECL-level data from the module immediately to its left and outputs ECL-level data to the module immediately to its right. Every module using the local bus is keyed to prevent two modules from fitting next to each other unless they are compatible. If using the local bus, select adjacent slots immediately to the left of the data-receiving module. The local bus can support up to nine VT1432B modules at full span at real time data rates. If the VXIbus is used, maximum data rates will be reduced, but the module can be placed in any available slot.
3. Using a small screwdriver or similar tool, set the logical address configuration switch on the VT1432B. (See Figure 1-1.) Each module in the system must have a unique logical address. The factory default setting is 0000 1000 (8). If a GPIB command module will be controlling the VT1432B module, select an address that is a multiple of 8. If the VXI system dynamically configures logical addresses, set the switch to 255.
4. Check the settings of the *Boot Source* and *ROM Programming* switches on the bottom of the module. Set switches 1 and 3 (BS1 and BS3) up with all the others switched down.

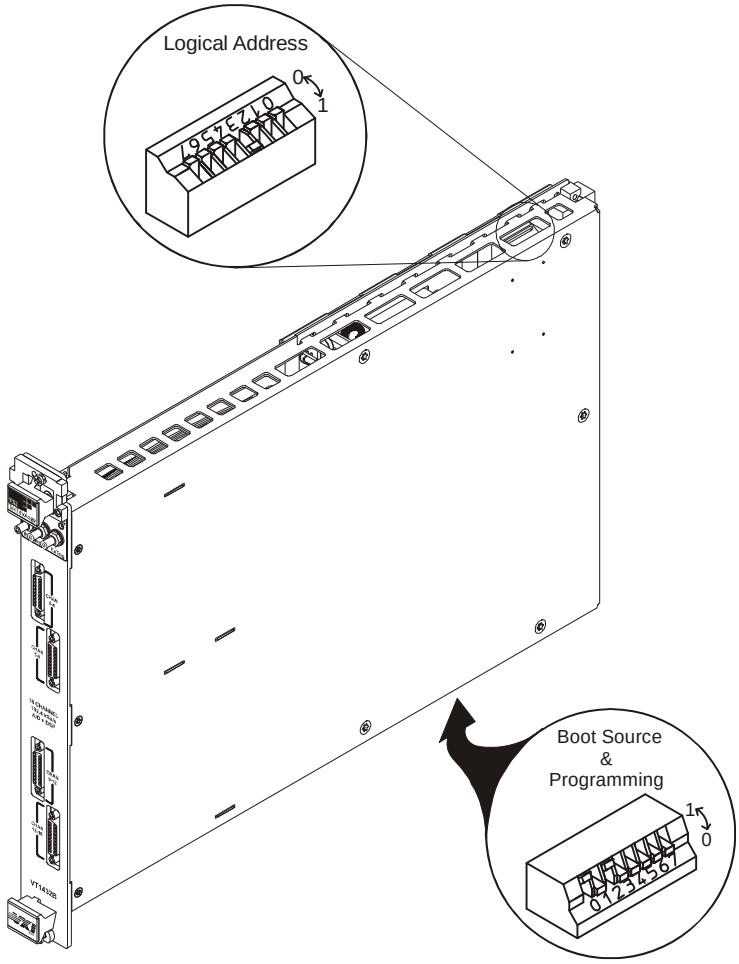


FIGURE 1-1: VT1432B SWITCH LOCATIONS

Set the mainframe's power switch to standby (⏻).

CAUTION	Installing or removing the module with power on may damage components in the module.

5. Place the module's card edges (top and bottom) into the module guides in the slot.
6. Slide the module into the mainframe until the module connects firmly with the backplane connectors. Make sure the module slides in straight.
7. Attach the module's front panel to the mainframe chassis using the module's captive mounting screws.

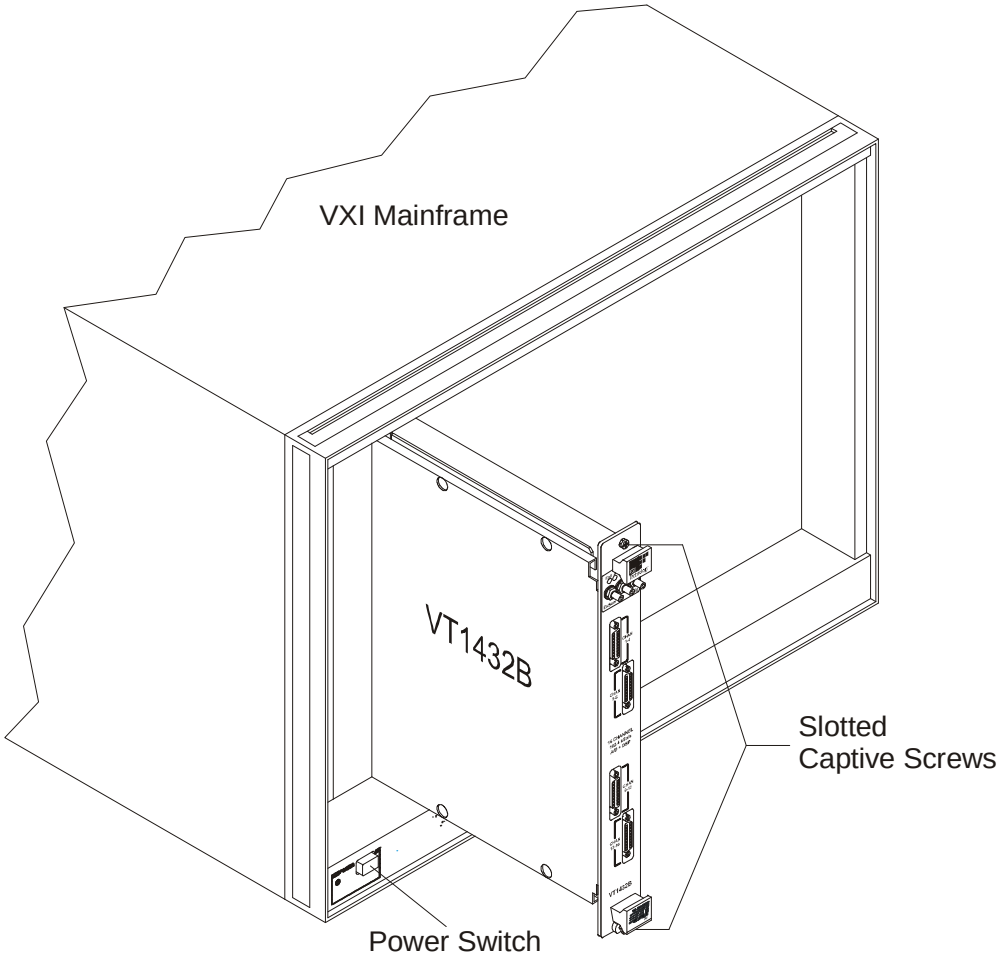


FIGURE 1-2: VT1432B CHASSIS INSTALLATION

MATING CONNECTORS

The VT1432B utilizes standard SMB connectors on its front panel. An example of an SMB cable mount connector which will couple with this connector is P/N: PE4046 (Pasternack Enterprises, Inc, CAGE: 53919), although other SMB cable mount connectors may be used.

INSTALLING THE HOST INTERFACE LIBRARIES

After the hardware has been assembled, the next step in installing a VT1432B is to install the host interface libraries. Refer to the section titled *Troubleshooting the VT1432B* to continue the installation process.

STORING THE MODULE

Store the module in a clean, dry, and static-free environment.

For other requirements, see storage and transport restrictions in *Specifications*.

TRANSPORTING THE MODULE

Package the module using the original factory packaging or packaging identical to the factory packaging.

Containers and materials identical to those used in factory packaging are available through VXI Technology offices.

If returning the module to VXI Technology for service, attach a tag describing the following:

- Type of service required
- Return address
- Model number
- Full serial number

In any correspondence, refer to the module by model number and full serial number.

Mark the container FRAGILE to ensure careful handling.

If it is necessary to package the module in a container other than the original packaging, observe the following (use of other packaging is not recommended):

- Wrap the module in heavy paper or anti-static plastic.
- Protect the front panel with cardboard.
- Use a double-wall carton made of at least 350 lb test material.
- Cushion the module to prevent damage.

CAUTION	Do not use styrene pellets in any shape as packing material for the module. The pellets do not adequately cushion the module and do not prevent the module from shifting in the carton. In addition, the pellets create static electricity that can damage electronic components.

SPECIFICATIONS

GENERAL SPECIFICATIONS	
FREQUENCY	
Sampling range	
maximum	102.4 kSa/s
minimum	2 Sa/s
Decimate by 5 and 2 filters provide lower sample rate settings. External sampling allows continuous settings from 102.4 kSa/s to 40.96 kSa/s.	
Frequency bandwidth	
maximum	46 kHz
minimum	244 µHz
FFT block size (samples)	32 to 8192
INPUT	
VT1432B/VT1436	16
VT1432B-1DE/VT1435	8
VT1432B-1DD, VT1435-1DD	4
Full-scale input ranges (in peak volts)	100 mV, 200 mV, 500 mV, 1 V, 2 V, 5 V, 10 V, 20 V. Add 23% to include over-range capability.
Input impedance	
differential	1 MΩ ‖ 110 pF nominal
either side-to-chassis	500 kΩ ‖ 220 pF nominal
single-ended mode	50 Ω nominal, (VT1435/VT1436 only, (-) terminal to GND)
AC coupling 3 dB corner frequency	< 1 Hz
CMRR (common mode rejection ratio)	
dc coupled (dc to 1 kHz)	> 63 dB
ac coupled (@ 1 kHz)	> 63 dB
maximum signal, either side-to-chassis	
5 V, 10 V, and 20 V range	±20 V peak
all other ranges	±10 V peak
Amplitude over-range detection	
over-range detection after common mode overload:	
5 V, 10 V, and 20 V range	±22.5 V
all other ranges	±10.5 V
differential overload	±130 ± 20% of range
over-voltage protection	42 V peak
DC residual	≤ ±1% of range ± 5 mV
AMPLITUDE	
Amplitude accuracy at 1 kHz	±0.7% of reading + (±0.01% of full-scale)
Flatness (relative to 1 kHz, at full-scale)	
dc to 42 kHz	
typical	±0.01 dB
worst case	1%
Amplitude resolution	24 bits (16 bits in some ranges for better data throughputs), less 2.3 dB over-range
CROSS-CHANNEL MATCH	
Cross-channel amplitude match	±0.01 dB (full-scale signal, Input ranges equal, frequency above 10 Hz if ac coupled
Cross-channel phase match	
2 V and 20 V ranges	± 0.1° at 1 kHz
all other ranges	$(f_{Hz} \times 6x10^{-5} + 0.1)°$
Phase match relative to tachometer	< 0.1° (typical)
DYNAMIC RANGE	
Spurious free dynamic range	-108 dBfs (typical) ((includes spurs, harmonic distortion, intermodulation distortion, alias products)
Crosstalk	< -104 dBfs (typical)
TRIGGER	
Trigger detection	digital
Trigger modes	input, external, source, TTL, TRG, RPM (with opt AYF)
VXI SYSTEM LEVEL FEATURES	
VXI standard information	Conforms to VXI revision 1.4 C-size, single slot width, register-based programming, "Slave" Data Transfer Bus functionality, A24 address capability, and D32 data capability. Optional Local Bus capability SUMBUS driver and receiver. Requires 2 or 4 TTLTRG lines for multi-module synchronization.

SOFTWARE	
Driver type	VXI*plug&play* C libraries with source code and ME4X ActiveX driver
Supported operating systems	MS Windows, Linux, HP-UX
***Plug&Play* compliance**	MS Windows, Linux, HP-UX

ARBITRARY SOURCE (1D4) SPECIFICATIONS

OUTPUT MODES	
	sine and pseudo random with burst and band translation, arbitrary waveform with loop or continuous output
FREQUENCY BANDWIDTH	
Sine, noise modes	
reconstruction filter bandwidth	0 Hz to 25.6 kHz
DSP data rate (f_s)	48.00 kHz to 65.636 kHz
data word size	16 bits
Arb modes	
reconstruction filter bandwidth	0 Hz to 6.4 kHz
data word size	20 bits
Signal output	
number of output channels	1
maximum amplitude	10 V peak, nominal
amplitude accuracy	±0.2 dB, 10 V peak to 0.158 V peak, 1 kHz sine wave in 200 Ω
harmonic distortion	< -70 dBc, 2 V to 10 V peak range, 0.05 to 1.00 scale factor, sine wave, ≥ 1 kΩ load
output impedance	< 0.5 Ω (typical)
maximum output current	100 mA (typical)
maximum capacitive load	0.01 µF (typical)
AMPLITUDE CONTROL	
Maximum amplitude	10 V peak nominal
Amplitude ranges	79 mV peak to 10 V peak in 0.375 dB steps
Amplitude scale factor	0.0 to 1.0, with 20-bit resolution
RESIDUAL DC OFFSET	
Offset after autozero	±2 mV
Offset after shutdown	±20 mV
Zeroing resolution	100 µV
OUTPUT OVERLOAD TRIP	
	> 17 V
AMPLITUDE RAMP DOWN TIME	
	0 s to 30 s (programmable)
SHUTDOWN	
Shutdown input	TTL levels
Shutdown time	5 s
Shutdown time, ac fail	< 4 ms

TACHOMETER INPUT (AYF) SPECIFICATIONS

TACHOMETER COUNTER	
	32-bit counter with roll-over detector bit
DECIMATE COUNTER	
	16-bit counter
INPUT SIGNAL TRIGGER LEVEL (TYPICAL)	
Voltage range	-25 V to +25 V
Resolution, levels < ±5 V	40 mV
Resolution, levels > ±5 V	200 mV
Hysteresis	0 mV to 250 mV (programmable)
Slope	positive or negative (programmable)
INPUT SIGNAL TIMING	
Maximum pulse width	5 µs
Maximum pulse rate	100 kHz
Trigger hold off	1 to 65536 clock periods
INPUT IMPEDANCE	
	20 kΩ (typical)

ENVIRONMENTAL SPECIFICATIONS	
OPERATING RESTRICTIONS	
Ambient temperature	0 °C to 55 °C
Humidity, non-condensing	20% to 90% relative humidity at 40 °C
Maximum altitude	4600 m (15,000 ft)
STORAGE AND TRANSPORT RESTRICTIONS	
Ambient temperature	-20 °C to 65 °C
Humidity, non-condensing	20% to 90% relative humidity at 40 °C
Maximum altitude	4600 m (15,000 ft)

POWER AND COOLING REQUIREMENTS								
VT1432A	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	4.90 A	0.60 A	0.03 A	0.19 A	0.05 A	0.38 A	0.45A	0.00 A
Dynamic Current	0.10 A	0.01 A	0.01 A	0.02 A	0.01 A	0.01 A	0.01 A	0.00 A
Cooling (10 °C Rise)	4.24 L/s, 0.33 mm H_2O							
VT1432B	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	6.00 A	0.19 A	0.03 A	0.40 A	0.04 A	0.47 A	0.47 A	0.00 A
Dynamic Current	0.66 A	0.02 A	0.01 A	0.02 A	0.02 A	0.03 A	0.02 A	0.00 A
Cooling (10 °C Rise)	4.94 L/s, 0.38 mm H_2O							
VT1432B-1DE	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	4.30 A	0.12 A	0.03 A	0.28 A	0.04 A	0.25 A	0.25 A	0.00 A
Dynamic Current	0.55A	0.02 A	0.02 A	0.02 A	0.02 A	0.03 A	0.02 A	0.00 A
Cooling (10 °C Rise)	3.19 L/s, 0.25 mm H_2O							
VT1432B-1DD	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	3.40 A	0.08 A	0.03 A	0.22 A	0.04 A	0.14 A	0.14 A	0.00 A
Dynamic Current	0.58 A	0.02 A	0.01 A	0.02 A	0.02 A	0.02 A	0.02 A	0.00 A
Cooling (10 °C Rise)	2.29 L/s, 0.18 mm H_2O							
VT1433A/B	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	5.50 A	0.95A	0.03A	0.56A	0.05A	0.44A	0.42 A	0.00 A
Dynamic Current	0.20 A	0.02 A	0.01A	0.02 A	0.01A	0.01A	0.01A	0.00 A
Cooling (10 °C Rise)	5.08 L/s, 0.51 mm H_2O							
VT1434A	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	4.90 A	0.60 A	0.03A	0.60 A	0.55A	0.20 A	0.25A	0.00 A
Dynamic Current	0.03A	0.03A	0.01A	0.04A	0.05A	0.01A	0.01A	0.00 A
Cooling (10 °C Rise)	4.39 L/s, 0.32 mm H_2O							
VT1435*	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	5.30 A	.12 A	0.03A	0.28A	0.04A	0.25A	0.25A	0.00 A
Dynamic Current	0.70 A	0.02 A	0.01A	0.02 A	0.02 A	0.02 A	0.02 A	0.00 A
Cooling (10 °C Rise)	3.61 L/s, 0.35 mm H_2O							
VT1436*	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	7.90 A	0.19A	0.03A	0.41A	0.04A	0.47A	0.47A	0.00 A
Dynamic Current	0.67A	0.02 A	0.01A	0.02 A	0.02 A	0.03A	0.02 A	0.00 A
Cooling (10 °C Rise)	5.76 L/s, 0.56 mm H_2O							
VT1435-1DD*	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	4.00 A	0.08A	0.03A	0.22 A	0.04A	0.14A	0.14A	0.00 A
Dynamic Current	0.68A	0.02 A	0.01A	0.02 A	0.01A	0.02 A	0.02 A	0.00 A
Cooling (10 °C Rise)	2.55 L/s, 0.25 mm H_2O							

** Listed current for +12 V and -5.2 V measured with IEPE current enabled, all inputs connected to IEPE sensors, and the individual channel range settings adjusted for linear operation with no over-voltage conditions. Unterminated inputs with IEPE current enabled and voltage range settings ≤10 V can cause +12 V current consumption to increase as much as 65% and -5.2 V current consumption to increase as much as 130%. Unterminated inputs should have their ranges set to 20 V to eliminate any possibility of excess current flow. +5 V current consumption will be as much as 25% less if IEPE current is disabled.*

POWER AND COOLING REQUIREMENTS - OPTIONS								
AYF (TACHOMETER)	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	0.14 A	0.00 A	0.00 A	0.00 A	0.00 A	0.10 A	0.06 A	0.00 A
Cooling (10 °C Rise)	0.38 L/s, 0.05 mm H_2O							
1D4 (SOURCE)	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	0.60 A	0.00 A	0.00 A	0.19 A	0.18 A	0.03 A	0.03 A	0.00 A
Cooling (10 °C Rise)	0.75 L/s, 0.12 mm H_2O							
VT3240 (AFV)	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A
Cooling (10 °C Rise)	External Device							
VT3241 (AFW)	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A	0.17 A	0.00 A	0.00 A
Cooling (10 °C Rise)	External Device							
VT3242 (CHARGE)	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A	0.26 A	0.22 A	0.00 A
Cooling (10 °C Rise)	External Device							
VT3243 (MICROPHONE)	**POWER**							
Voltage	+5 V	-5.2 V	-2 V	+12 V	-12 V	+24 V	-24 V	+5 V STDBY
DC Current	0.00 A	0.00 A	0.00 A	0.00 A	0.00 A	0.25 A	0.15 A	0.00 A
Cooling (10 °C Rise)	External Device							

SECTION 2

GETTING STARTED WITH THE VT1432B

INTRODUCTION

This section provides assistance in getting the VT1432B, VT1435, and VT1436 modules running and making simple measurements. It shows how to install the VXI*plug&play* Library and how to run some of the example programs that are included. The VXI*plug&play* Library communicates with the hardware using VISA (Virtual Instrument Software Architecture). VISA is the input/output standard upon which all the VXI*plug&play* software components are based. The library is compatible with Microsoft® Windows® operating systems (see *System Requirements* in this section for details). For more information, see *Where to Get More Information* in *Section 3*.

System Requirements

- An IBM-compatible personal computer with either Windows 2000, Windows XP, or later. (With any Windows OS, use the VXI*plug&play* library.)
- Additional hardware and software to connect the IBM compatible computer to a VXI mainframe.
- Software is supplied on CD-ROM.

VXIplug&play Drivers and Product Manuals CD

The *VXI*plug&play *Drivers and Product Manuals* CD-ROM is shipped with the VT1432B module. This CD includes the VT1432B VXI*plug&play* host interface library for Windows operating systems with associated examples and the user's manual.

Getting Updates

The latest version of the VT1432B instrument drivers can be found on-line at *www.vxitech.com*.

INSTALLING THE VXI*PLUG&PLAY* DRIVERS

1) Insert the *VXI*plug&play *Drivers and Product Manuals* CD into the CD-ROM drive.
2) Navigate to <CD-ROM>:\Drivers\DAQ Drivers\. Double click on driver_vxipnp_vt1432_b_07_04.exe (or later) to begin installation of the driver suite.
3) The *Welcome* dialogue box will appear. Click **Next** to continue.
4) The *Select Components* dialogue box appears next. Choose the drivers to be installed. Once the required drivers are selected, click **Next**.
5) The *Choose VXI PnP Location* dialogue box appears next. The default destination folder is determined by the VISA version previously installed on the PC. If no VISA software has been previously installed, the default destination folder is C:\Program Files\VISA\winnt. To change the location, click **Browse** and choose a new folder location. Click on **Next** to continue.
6) The *Choose ME COM Driver Location* dialogue box will appear. The default destination folder is C:\Program Files\VXI Technology\ME. To change the location, click **Browse** and choose a new folder location. Click on **Next** to continue.
7) The *Select Program Manager Group* dialogue box appears providing the opportunity to change the name of the program folder that will be created in the Start Menu. The default name is "VXI Technology." Click **Next** to continue.
8) The *Start Installation* dialogue box appear next. Click on **Next** to begin installation.
9) After the program files load, the *Installation Complete* dialogue box will appear. Click *Finish* to complete the installation process.

The Resource Manager

The Resource Manager is a program from the hardware interface manufacturer. It looks at the VXI mainframe to determine what modules are installed. It should be run every time the system is powered up. If a "No VT1432-36 can be found in this system" message appears from the VT1432B/35/36 soft front panel, run the Resource Manager.

Before running the VT1432B software, make sure that the hardware is configured correctly and that the Resource Manager runs successfully. Before using the measurement system, all of its devices must be set up, including setting the addresses and local bus locations. No two devices can have the same address. Usually addresses 0 and 1 are taken by the Resource Manager and are not available.

For more information about the Resource Manager, see the hardware interface documentation.

THE VXI*PLUG&PLAY* SOFT FRONT PANEL

Using the soft front panel

If the VT1432B software is run in a Windows environment, the soft front panel (SFP) program can be used as an interface.

The soft front panel can be useful for checking the system to make sure that it is installed correctly and that all of its parts are working. However, it is not very useful for making measurements. It cannot be controlled from a program and it does not access all of the VT1432B's functionality.

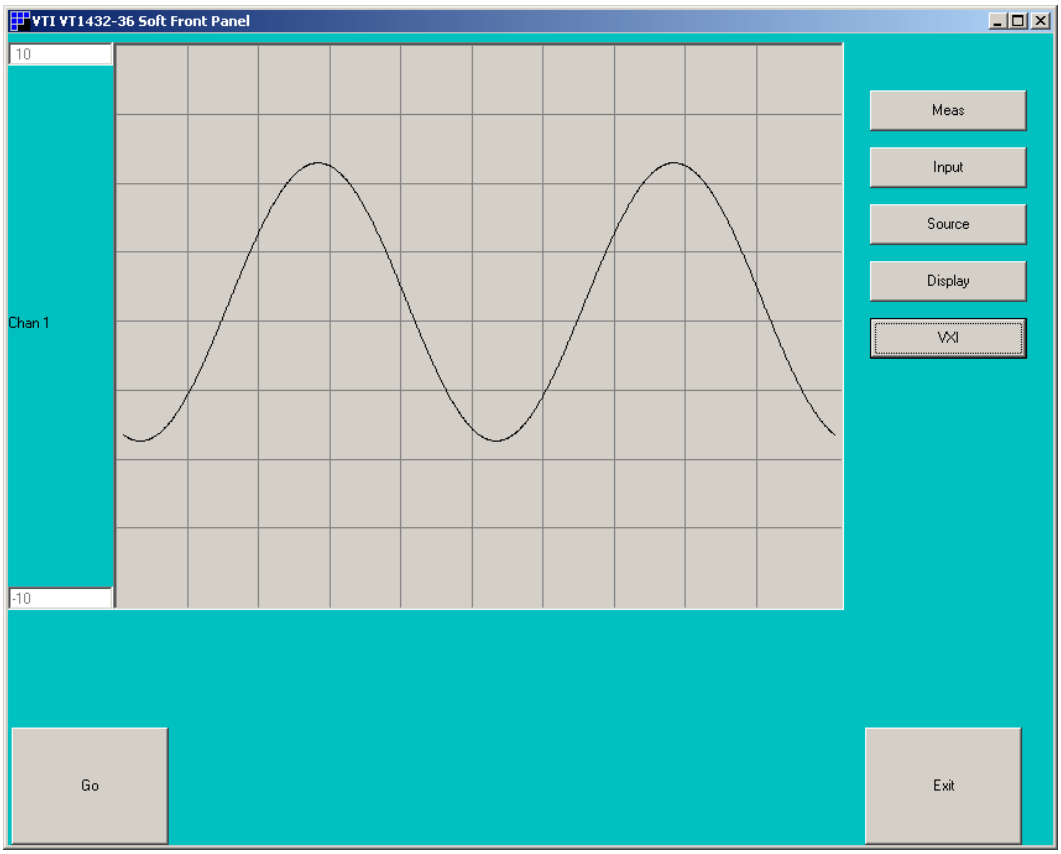


FIGURE 2-1: THE SOFT FRONT PANEL INTERFACE

The buttons on the right side of the SFP display are defined as follows:

Meas

This button opens the Measurement Control dialog box that sets:

- Measurement single/repeat
- Mode block/continuous
- Trigger auto/manual/input
- Frequency span
- Block size

Input

This button opens a dialog box that sets up the VT1432B's inputs and configures:

- Channel number
- Range
- Coupling, ac or dc
- Grounding method
- Digital anti-alias filter
- Analog anti-alias filter
- Trigger on/off
- Trigger mode level/bound
- Trigger level
- Hysteresis
- Trigger Slope

There is a checkbox to make all channels identical.

Source

This opens a dialog box for controlling the source output of the VT1432B's source. This is only available for VT1432B's that have the arbitrary source option, 1D4. This sets:

- Channel number
- Active on/off
- Mode sine/burst sine/random/burst random
- Ramp rate
- Sine frequency
- Sine phase
- Output normal/grounded/open/cal/multi
- COLA (Constant Output Level Amplifier) off/on
- Duty Cycle
- Sum off/on
- Seed
- Range

Display

This button opens a dialog box that specifies how the data will be displayed. For each trace, an input channel (or OFF) and an output file can be specified.

VXI

This button opens a dialog box showing the modules installed in the VXI mainframe and indicating which are active and inactive. The "resource name" for each module is the interface card name that has been assigned to it.

Go

Use the Go button to start the measurement.

Exit

Use the Exit button to exit the soft front panel.

SECTION 3

USING THE VT1432B

INTRODUCTION

This section shows how to use the VT1432B using the VXI*plug&play* Host Interface Library.

The host interface library for the VT1432B is a set of functions that allow the user to program the register-based VT1432B at a higher level than register reads and writes. The library allows groups of VT1432Bs to be set up and programmed as if they were one entity. It is compatible with Windows operating systems and communicates with the hardware using VISA. VISA is the input/output standard upon which VXI*plug&play* software components are based.

The library includes routines to set up and query parameters, start and stop measurements, read and write data, and control interrupts. Routines to aid debugging and perform low-level I/O are also included.

For information on diagnostics, see *Troubleshooting the VT1432B*.

WHAT IS VXI*PLUG&PLAY*?

VXI Technology uses VXI*plug&play* technology in the VT1432B. This section outlines some of the details of VXI*plug&play* technology.

Overview

The fundamental idea behind VXI*plug&play* is to provide VXI users with a level of standardization across different vendors well beyond what the VXI standard specification spells out. The VXI*plug&play* Alliance specifies a set of core technologies centering on a standard instrument driver technology.

VXI Technology offers VXI*plug&play* drivers for VEE-Windows. The VXI*plug&play* instrument drivers exist relative to so-called "frameworks." A framework defines the environment in which a VXI*plug&play* driver can operate. The VT1432B has VXI*plug&play* drivers for Windows frameworks.

NOTE	The VXI*plug&play* drivers for the VT1435 and VT1436 are incorporated into the VT1432-based driver suite. Most prefixes for the driver calls are "vt1432_" based, but also apply to the VT1435 and VT1436 modules. However, the vt1432_readTEDS and vt1432_writeTEDS function calls can only be used on the VT1435 and VT1436 modules with the TEDS option installed.

VXIplug&play drivers

The VT1432B VXI*plug&play* driver is based on the following architecture:

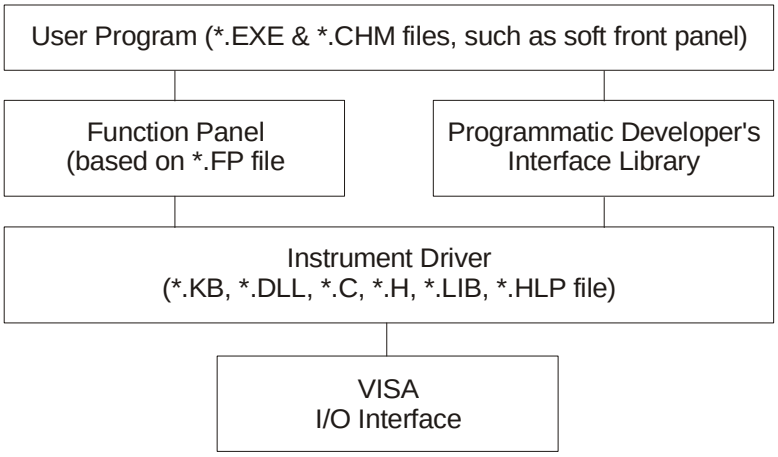


FIGURE 3-1: VXI*PLUG&PLAY* DRIVER ARCHITECTURE

It is most useful to discuss this architecture from the bottom up.

The VISA I/O interface allows interoperability of the VXI*plug&play* driver technology across interfaces.

The actual instrument driver itself is a DLL (Dynamic Linked Library) created from:

- A set of source (*.C) files.
- A set of header (*.H) files, used for compiling the file as well as to describe the driver's calls to any program using the driver.
- A standard driver library (*.LIB) file, to provide the standard functionality all the drivers would require.

This DLL is a set of calls to perform instrument actions — at heart, that is all a VXI*plug&play* driver is — a library of instrument calls.

This driver is accessed by Windows applications programs written in languages such as Visual C++ or Visual BASIC, using programming environments such as VEE or NI LabView™.

A Windows Help (*.chm) file is included which provides descriptive information and code samples for the functions in the VXI*plug&play* DLL. This help file can be viewed in the standard Windows Help viewer.

The Soft Front Panel

The soft front panel is a stand-alone Windows application, built on top of the VXI*plug&play* driver DLL; it is used for instrument evaluation and debugging and as a demo. It is not a programmable interface to the instrument, nor can it be used to generate code.

The soft front panel also accesses the same Windows Help file as provided with the DLL.

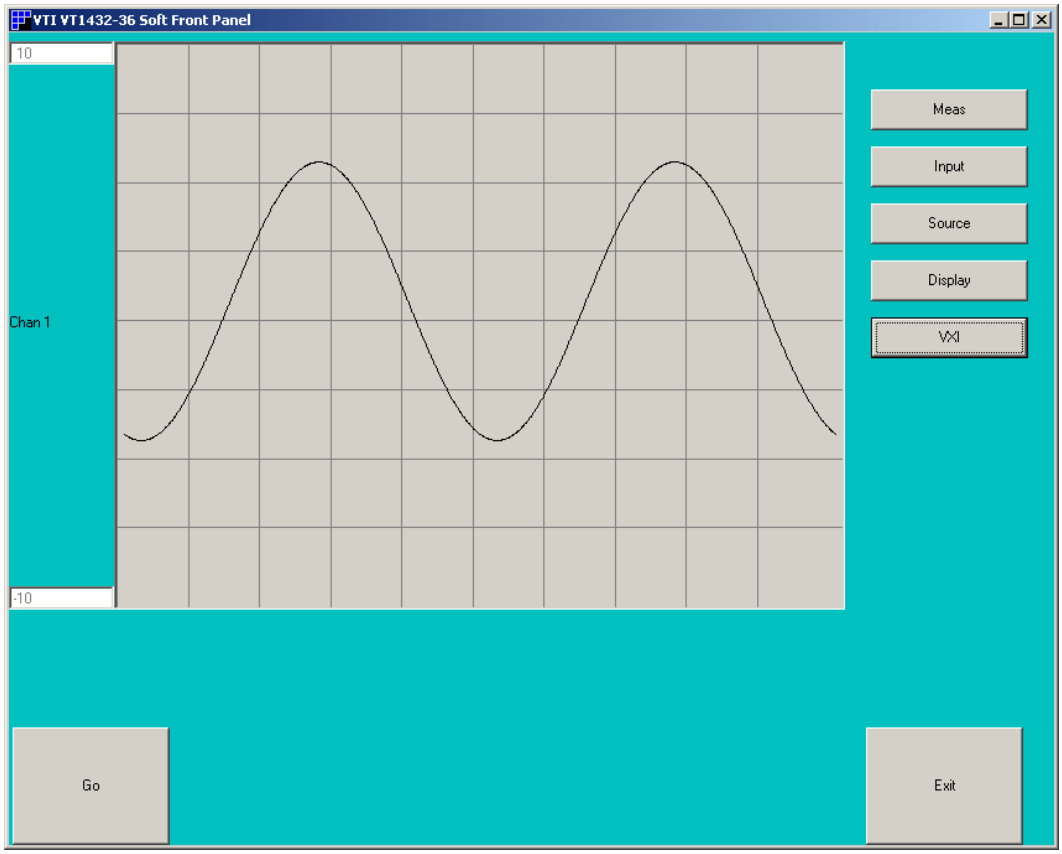


FIGURE 3-2: AN EXAMPLE OF A SOFT FRONT PANEL (SFP)

HEADER AND LIBRARY FILES

In a Windows environment, the following directories/files are in the directory *<VXIPNP>:

KBASE \ vt1432.kb	Knowledge base file
winNT \ Bin \ vt1432_32.dll	The VXI*plug&play* driver
winNT \ Include\ vt1432.h	Header for linking to the VXI*plug&play* driver
winNT \ Lib \ Msc \ vt1432_32.lib	Lib for linking C programs to VXI*plug&play*

The following files are in the directory *<Vxipnp>\winnt\VT1432:

vt1432.exe	Soft front panel program
vt1432.bas	header for Visual Basic
vt1432.fp	The “FP” file used by VEE and CVI
vt1432.hlp	Windows help file
Read.me	The latest information for the product
examples \ vb *	Visual Basic example programs
examples \ c *	C example programs
lib \ sema.bin	Firmware program for the VT1432B
lib \ sfp.ico	Icon for help file
lib \ sinewave.ico	Icon for soft front panel
source \ *	Source files for vt1432_32.dll

**where <VXIPNP> is typically C:\VXIPNP or C:\Program Files\VISA*

VT1432B AND E1432 LIBRARY COMPATIBILITY

The following table lists similar library calls that existed in the Agilent/HP E1432. It provides the name of the former Agilent/HP call, the present VXI Technology, Inc. call, and a brief description of the call's function.

VT1432B	E1432A	Location	Description
vt1432_32.dll	hpe1432_32.dll	*<VXIPNP>\winnt\bin	*plug&play* library DLL
vt1432_32.lib	hpe1432_32.lib	<VXIPNP>\winnt\lib\msc	import library DLL
vt1432.h	hpe1432.h	<VXIPNP>\winnt\include	include file for C-programming
vt1432.bas	hpe1432.bas	<VXIPNP>\winnt\include	include file for visual basic programming
vt1432.dll	hpe1432.dll	<VXIPNP>\winnt\VT1432 (or HPE1432)\examples\matlab	Matlab MEX DLL for Matlab users.
*where <VXIPNP> is usually C:\VXIPNP or C:\Program Files\VISA			

Instruments Supported by the VT1432B library include: E1432A, E1433A/B, E1434A, VT1432A, VT1432B, VT1433B, VT1434A, VT1435, and VT1436.
Instruments Supported by the E1432 library include: E1432A, E1433A/B, E1434A, VT1432A, VT1433B, and VT1434A.

In addition to the files listed above, the VT1432 *plug&play* library has the hpe1432.h and hpe1432.bas include files from the E1432 library. This allows VT1432 (35/36) users to use application programs that were written for the Agilent/HP E1432 VXI *plug&play* library. By using these include files, the user can compile and link existing source programs that have hpe1432_xxxx() API calls. C-programmers can use vt1432_32.lib to link the library.

For existing applications that are dependent on previous hpe1432_32.dll or hpe1432.dll (Matlab), the user is able to run these applications without recompiling the source code. Simply rename the "vt1432_32.dll" file as "hpe1432_32.dll" (or "vt1432.dll" as "hpe1432.dll").

CHANNELS AND GROUPS

This section provides information related to using channels and groups. For more detailed information, see the VT1432B help text.

Channel Groups

In the VT1432B VXI*plug&play* driver, a channel group is the basic unit of hardware control. To control any channel, it must first be assigned to a group with the vt1432_createChannelGroup function. In addition to creating the group, this function returns a "handle" that uniquely identifies the group. This handle can then be used to direct functions to all channels in the group.

When a channel group is created, all input and tachometer channels in the group are automatically activated and all source channels are de-activated. However, when deleted, the input and tachometer channels are not automatically de-activated. Any input or tachometer channel that remains active after its group is deleted will continue to supply data to its module's FIFO buffer during a measurement—consuming module resources. For this reason, channels should always be explicitly de-activated in a group before deleting them. Channels can be de-activated with the vt1432_setActive command. Delete channel groups with vt1432_deleteChannelGroup and vt1432_deleteAllChanGroups.

In addition, when creating a channel group, channels which are not mentioned in the new group are not turned off. Any channels that are not to be active must be explicitly de-activated. (An exception is a power-up, when only the channels in the initial channel group are active.)

Initialization

The command used to initialize the system is vt1432_init. This function initializes the VXI*plug&play* library and registers all VT1432B modules. It also checks the existence of a VT1432B module at each of the logical addresses given in the resource list and allocates logical channel identifiers for each channel in all of the VT1432Bs. Input channels, source channels, and tachometer/trigger channels are kept logically separated.

Most other functions cannot be used until after vt1432_init, but there are two functions that can be used before initialization to get information needed by vt1432_init. These are vt1432_find and vt1432_getHWConfig. The vt1432_find function searches the VXI mainframe and returns the VXI Logical Address for every VT1432B found. The vt1432_getHWConfig function returns additional information about the hardware.

After vt1432_init is run, use vt1432_getNumChans to get the total count of inputs, sources, and tachs for all VT1432B modules named in the vt1432_init call.

Creating a Channel Group

The function vt1432_createChannelGroup creates and initializes a channel group. A channel group allows commands to be issued to several VT1432B channels at once, simplifying system setup. Channel groups can overlap. The state of an individual VT1432B channel that is in more than one channel group is determined by the most recent operation performed on any group to which this channel belongs.

As a side effect, this function makes all input and tachometer channels in the channel group active and all source channels in the channel group inactive. This function does not inactivate other channels within the modules that the channels are in and does not preset the channels in the new group.

After a channel group has been created, use vt1432_getGroupInfo to get selected information about the group. It is possible for vt1432_getGroupInfo to be set up to return the number of modules, channels, inputs, sources, or tachs in the group. It can also return a list of the modules, channels, inputs, sources, or tachs.

Input, Source, and Tachometer Channels

Channel numbers must fall in particular ranges for different types of channels. Input channel numbers range from 1 to 4,095. Source channel numbers range from 4,097 to 8,191. Tachometer channel numbers range from 8,193 to 12,287.

A mixture of input, source, and tachometer channels may exist in one group. However, it is also important for many functions to be sent only to the appropriate type of channel. For example, asking for a blocksize from a tachometer channel can cause an error. It may be useful to set up several channel groups at the beginning of the program: one for input channels, one for source channels, one for tachometer channels, and one that combines all three channel types. The input handle could be used for input-only functions, the source for source-only functions, and the tachometer handle for tachometer-only functions. The “all-channels” handle could then be used for all other functions.

MULTIPLE-MODULE/MAINFRAME MEASUREMENTS

Grouping of Channels/Modules

The interface library for the VT1432B is designed to allow programming of several channels from one or several distinct modules, as if they were one entity. Each VT1432B module has up to 16-channels. The library may control up to a maximum of 255 VT1432B modules (4,080 channels).

The function vt1432_createChannelGroup can be used to declare any number of groups of channels, possibly overlapping. Each group can be uniquely identified by a group ID.

The 'target' of a library function is either a channel, a group or (rarely) a module, depending on the nature of the call. When the same library function may be called with either a channel or a group identifier, its 'target' is shown by a parameter named ID.

Multiple-Module Measurements

A channel group that spans more than one module will need to be configured to use the TTL trigger lines on the VXI bus for inter-module communications. This configuration is automatically performed in the vt1432_initMeasure call unless defeated using vt1432_setAutoGroupMeas.

The following discussion outlines what vt1432_initMeasure does automatically. This must be done by the user if vt1432_setAutoGroupMeas has been used to defeat auto configuration.

There are eight VXI TTL trigger lines that can be used for multi-module synchronization. Often, these lines are used in pairs: one for sample clock and one for Sync/Trigger. The vt1432_setTtltrgLines function selects which TTL trigger lines to use; this function always uses the TTL trigger lines in pairs. Calling vt1432_setClockSource with the group ID will set all modules to the same pair.

All modules need to be set to use the shared sync line rather than the default setting of internal sync. This can be done with the vt1432_setMultiSync function, using the group ID.

One module of the set of modules needs to be set to output the sync pulse. The module with the lowest VXI logical address is called the "system module" and is assigned this duty. This can be set with the vt1432_setMultiSync function call, using the lowest channel ID in the group (NOT the group ID).

All modules except the "system module" need to be set to use the VXI TTL trigger lines as the clock source. Use vt1432_setClockSource for this.

Set the "system module" to output the clock. Use vt1432_setClockMaster for this. After this is done, all system sync pulses come from the "system module" and drive the measurement state machines on all boards in the group.

Possible Trigger Line Conflict

The following describes a scenario where VT1432B modules might conflict and prevent a proper measurement. The conditions allowing the conflict are complex, but should be understood by the user to help avoid any conflicts.

After a measurement has completed, the modules are left set up. If a module (call it module 'A') is driving the TTL trigger lines and a different group is started which also drives the TTL trigger lines (and that different group does not include module 'A'), then module 'A' will conflict and prevent the other group from functioning. In this case, make a call to vt1432_finishMeasure (using the old group ID which includes 'A') to turn off module 'A' and allow the new group to function.

Note that if the new group includes all modules of the old group, the conflict will not occur, as vt1432_initMeasure will reset all modules as needed. Also, note that single-module groups do not drive the TTL trigger lines, so single-module groups are immune to this conflict.

Managing Multiple-mainframe Measurements

In a single-mainframe measurement, the VT1432B communicates with other VT1432Bs through the TTLTRG lines. However, when using the VXI-MXI bus extender modules, the TTLTRG lines, which carry the group synchronization pulse and sample clock, are extended only in one direction. This unidirectional signal connection restricts the types of measurements that can be made in a multiple mainframe environment.

The following types of multiple mainframe measurements cannot be performed:

- Unequal pre-trigger delay settings between mainframes
- Channel triggering by channels in Mainframe B
- Lower spans or longer blocksizes in Mainframe B
- Different digital filter settling times between VT1432B modules

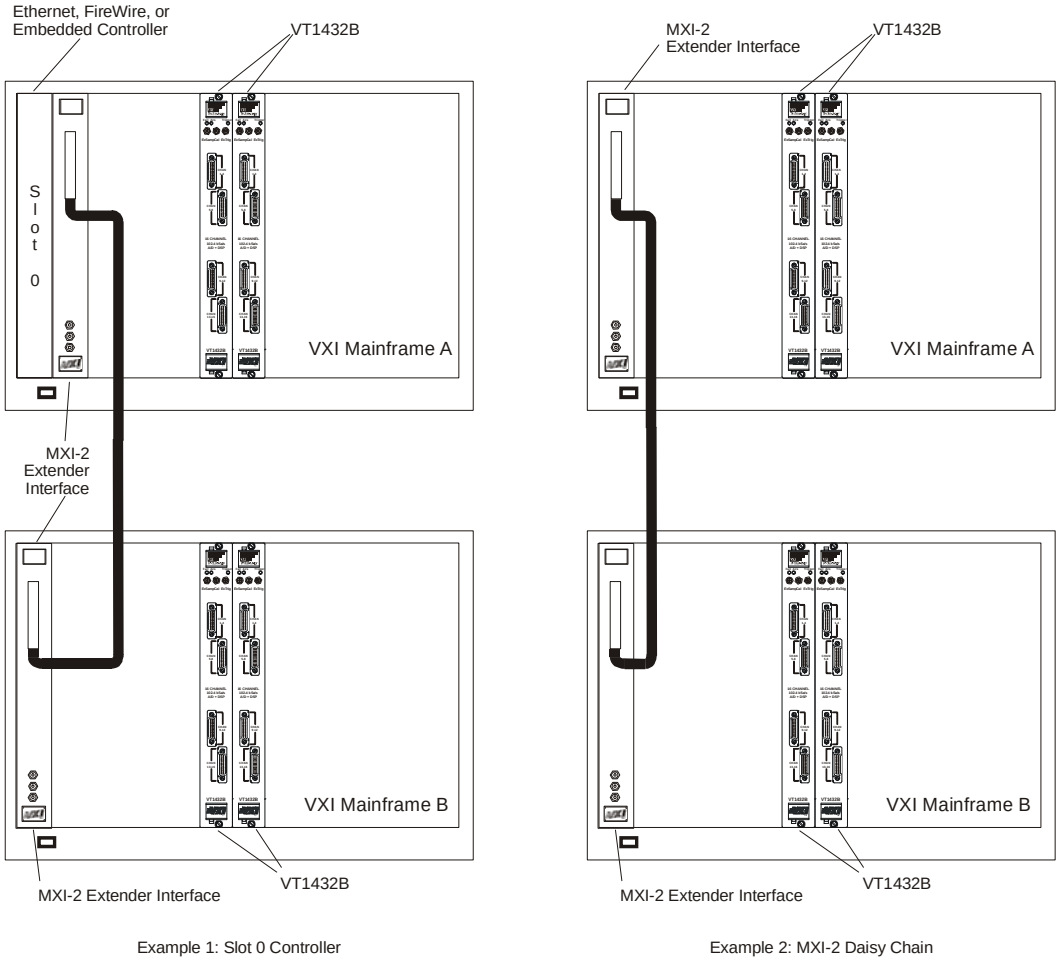


FIGURE 3-3: MULTIPLE MAINFRAMES – TWO MAINFRAMES

In the Example 1 above, mainframe A contains the Slot 0 embedded controller for a multiple mainframe system. Mainframe A is connected to mainframe B with a MXI-2 extender interface. In Example 2, a MXI-2 daisy chain configuration is used. To manage this multiple mainframe environment successfully, use the following guidelines.

- Locate modules with logical addresses less than 128 in mainframe A.
- Locate modules with logical addresses greater than 127 in mainframe B.
- Locate the highest-numbered channels in mainframe A.
- Locate the last module in the module list specified in the call to vt1432_init in mainframe A.
- Locate the module that generates the group synchronization pulse in mainframe A.
- Locate the channels performing channel triggering in mainframe A.
- Locate the module with the shared sample clock in mainframe A.

- If a groupID is not used with the call vt1432_readRawData or vt1432_readFloat64Data, empty the VT1432B's FIFOs in Mainframe B before mainframe A. In other words, do not empty the FIFOs in Mainframe A unless the FIFOs in mainframe B have been emptied. For more information about groupID see *Grouping of Channels/Modules* in this section.
- If more than two mainframes are needed, daisy-chain them together. Treat each mainframe after the first as a mainframe B. See the example on the next page.

Phase Performance in Multiple Mainframe Measurements

Phase specifications are degraded by the delay that the inter-mainframe interface gives the sample clock. This delay is insignificant for many low-frequency applications because the phase error is proportional to frequency. A system with two VXI-MXI modules and a 1 m cable, typically has a 76 ns sample clock delay in Mainframe B. This corresponds to an additional 0.007 degree phase error at 256 Hz and an additional 0.55 degree phase error at 20 kHz.

Using a 4 m cable (which adds approximately 18 ns of delay) causes a total of 94 ns clock delay in Mainframe B. This corresponds to an additional 0.0087 degree phase error at 256 Hz and an additional 0.68 degree phase error at 20 kHz.

The cable adds approximately 6 ns per meter of cable.

Each daisy-chained mainframe adds another increment of delay, but only for the additional cabling length.

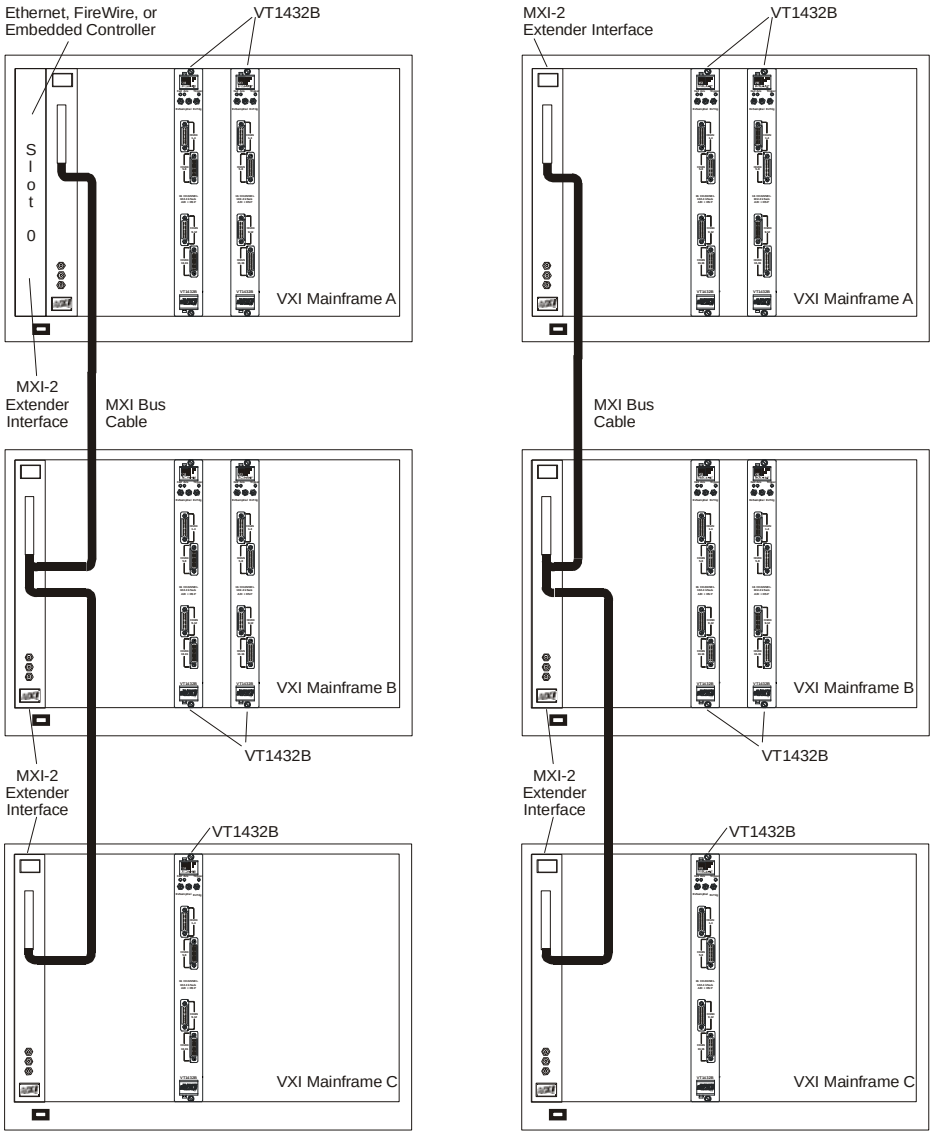


FIGURE 3-4: MULTIPLE MAINFRAMES – THREE MAINFRAMES

Synchronization in Multiple-mainframe Measurements

A TTL trigger line between VT1432Bs making group measurements keeps all modules synchronized. This is an open-collector line where each module holds the one designated as the SYNC line low until the module is ready to advance to the next measurement state. Another TTL Trigger line is designated to carry the sample clock to all modules. This shared sample clock may come from any VT1432B module in Mainframe A or from an external signal routed through the Slot 0 Commander in mainframe A.

One module is responsible for pulling the SYNC line low to start each group's state transition. Then, each module holds the line low until it is ready. When all modules are ready, the SYNC line drifts high. The unidirectional line prevents modules in Mainframe B from holding-off modules in Mainframe A.

The lowest logical address must be in mainframe A due to VXI-MXI and Resource Manager (RM) constraints. Group constraints with the VXI*plug&play* Library force modules in Mainframe A to have their FIFOs emptied last. The VXI*plug&play* library reads data in channel order, so the highest channel is read last. To get this to work automatically, the call to vt1432_init must list the logical addresses in descending order.

Channel triggering must be done only by modules in mainframe A. A trigger in any other mainframe would not be communicated back on the SYNC line to Mainframe A. The Library itself selects the VT1432B with the highest channel number for synchronization.

VXI-MXI Module Setup and System Configuration

The VXI-MXI Module setup in Mainframe A needs to be changed from those set by the factory. The VXI-MXI module is not the Slot 0 Controller for mainframe A. Refer to the VXI-MXI2 user's manual for configuration settings. This requires changing several switch settings.

- Set the module as not being the Slot 0 Controller.
- Set the VME timeout to 200 µs.
- Set the VME BTO chain position to 1 extender, non-slot 0.
- Do not source CLK10.
- Set the proper logical address.

MODULE FEATURES

Data Flow Diagram and FIFO Architecture

Figure 3-5 shows data flow in the VT1432B. In this example, there are four 4-channel input assemblies for a total of 16 input channels. The data for all channels is sent to the FIFO. The FIFO is divided into sections, one for each channel. The data moves through a circular buffer (first-in-first-out) until a trigger causes it to be sent on to the VME Bus. The data can also be sent to the Local Bus if option UGV is present.

The size of the sections in the FIFO is flexible. The amount of DRAM memory for each channel is the total DRAM memory divided by the number of channels. The DRAM size is 32 MB.

The trigger can be programmed to trigger on the input or on information from the software. The following are examples of ways a trigger can be generated:

- input level or bound
- source
- external trigger
- RPM level (with tachometer option AYF)
- ttl_trigger (VXI backplane)
- free-run (automatic)

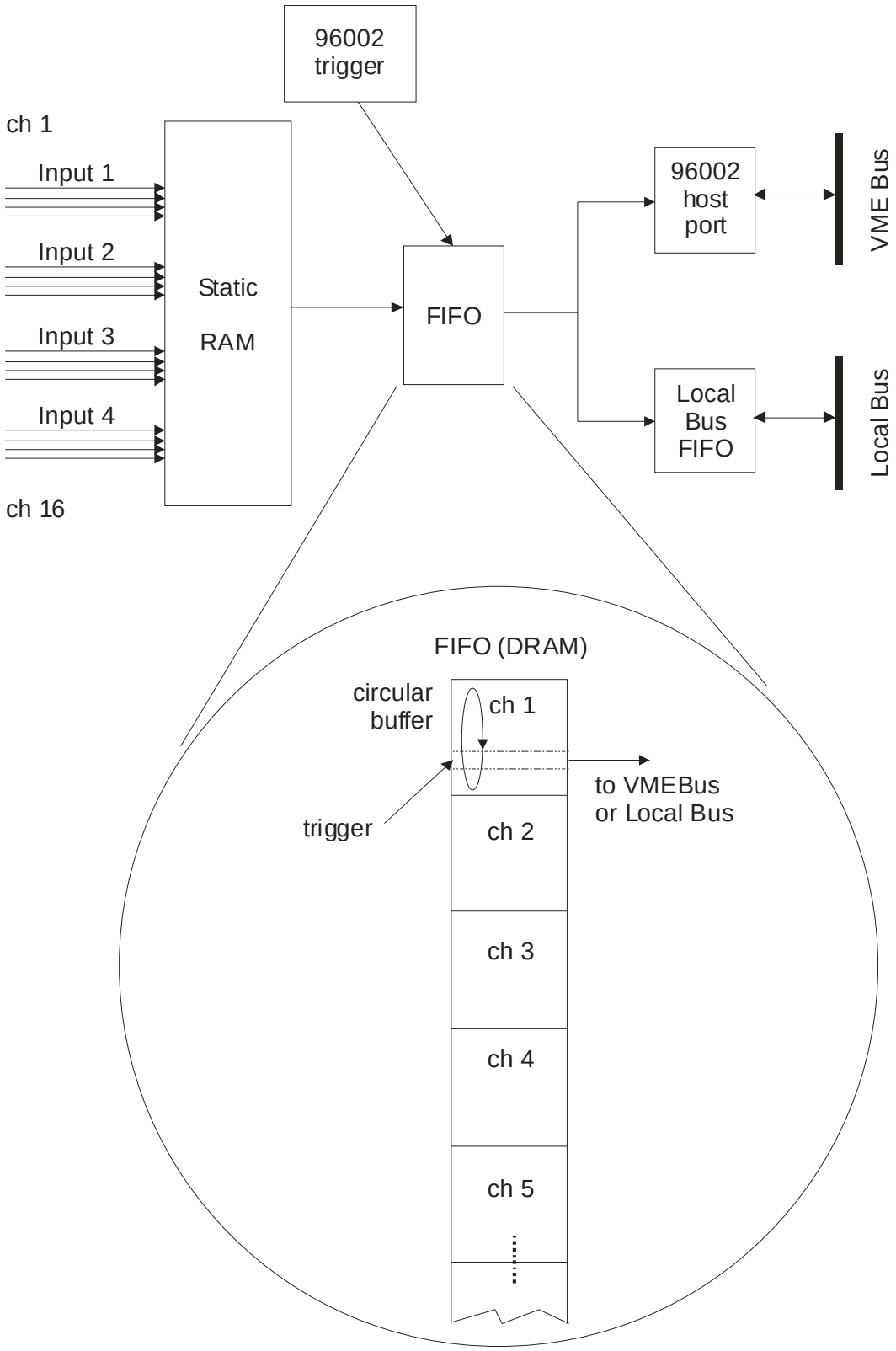


FIGURE 3-5: DATA FLOW AND FIFO ARCHITECTURE

Base Sample Rates

Baseband Measurement Spans

Table 3-1 on page 37 shows the measurement spans available for base sample rates for baseband measurements.

In this table, "f_s" is the sample frequency or sample rate. The value for zero divide-by-two steps and no divide-by-5 step is the top measurement span corresponding to the sample rate. This is with no decimation and using 400 lines to avoid alias. The other values on the table are for this top span decimated by five and/or two.

For a VT1432B which has the arbitrary source option, 1D4, the sample rate for the source is automatically set to be the same as the sample rate selected for the inputs. When the source is active, the sample rate cannot be greater than 65.536 kHz.

Decimation Filter Diagram

Figure 3-6 illustrates the way the spans in the table are generated. In the case of baseband spans (lower limit of span fixed at zero), the frequency can (optionally) be divided by five and then (optionally) divided by two up to eight times.

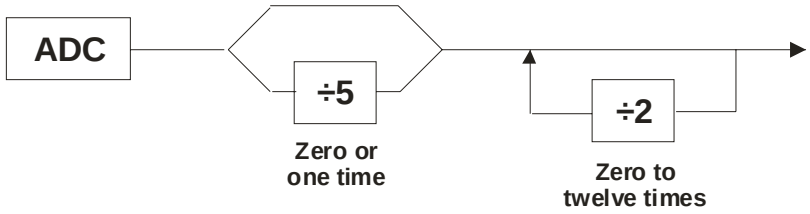


FIGURE 3-6: DECIMATION FILTER DIAGRAM – BASEBAND

Sample Freq. (f_s)	40,960		48,000		50,000		51,200		64,000	
# of ÷ 2 steps	with ÷5	w/o ÷5	with ÷5	w/o ÷5	with ÷5	w/o ÷5	with ÷5	w/o ÷5	with ÷5	w/o ÷5
0	3200	16000	3750	18750	3906.25	19531.25	4000	20000	5000	25000
1	1600	8000	1875	9375	1953.125	9765.625	2000	10000	2500	12500
2	800	4000	937.5	4687.5	976.5625	4882.813	1000	5000	1250	6250
3	400	2000	468.75	2343.75	488.2813	2441.406	500	2500	625	3125
4	200	1000	234.375	1171.875	244.1406	1220.703	250	1250	312.5	1562.5
5	100	500	117.1875	585.9375	122.0703	610.3516	125	625	156.25	781.25
6	50	250	58.59375	292.9688	61.03516	305.1758	62.5	312.5	78.125	390.625
7	25	125	29.29688	146.4844	30.51758	152.5879	31.25	156.25	39.0625	195.3125
8	12.5	62.5	14.64844	73.24219	15.25879	76.29395	15.625	78.125	19.53125	97.65625
9	6.25	31.25	7.324219	36.62109	7.629395	38.14697	7.8125	39.0625	9.765625	48.82813
10	3.125	15.625	3.662109	18.31055	3.814697	19.07349	3.90625	19.53125	4.882813	24.41406
11	1.5625	7.8125	1.831055	9.155273	1.907349	9.536743	1.953125	9.765625	2.441406	12.20703
12	0.78125	3.90625	0.915527	4.577637	0.953674	4.768372	0.976563	4.882813	1.220703	6.103516

Sample Freq. (f_s)	65,536		80,000		100,000		102,400	
# of ÷ 2 steps	with ÷5	w/o ÷5	with ÷5	w/o ÷5	with ÷5	w/o ÷5	with ÷5	w/o ÷5
0	5120	25600	6250	31250	7812.5	39062.5	8000	40000
1	2560	12800	3125	15625	3906.25	19531.25	4000	20000
2	1280	6400	1562.5	7812.5	1953.125	9765.625	2000	10000
3	640	3200	781.25	3906.25	976.5625	4882.813	1000	5000
4	320	1600	390.625	1953.125	488.2813	2441.406	500	2500
5	160	800	195.3125	976.5625	244.1406	1220.703	250	1250
6	80	400	97.65625	488.2813	122.0703	610.3516	125	625
7	40	200	48.82813	244.1406	61.03516	305.1758	62.5	312.5
8	20	100	24.41406	122.0703	30.51758	152.5879	31.25	156.25
9	10	50	12.20703	61.03516	15.25879	76.29395	15.625	78.125
10	5	25	6.103516	30.51758	7.629395	38.14697	7.8125	39.0625
11	2.5	12.5	3.051758	15.25879	3.814697	19.07349	3.90625	19.53125
12	1.25	6.25	1.525879	7.629395	1.907349	9.536743	1.953125	9.765625

* For the top span, the bandwidth is 1.16 times span shown.

TABLE 3-1: TABLE OF BASEBAND MEASUREMENT SPANS (HZ)

Additional Notes on Measurement Spans

The minimum span is approximately is 8 Hz, where the maximum span is 40 kHz.
Top span 46,400 Hz = 464 lines.

To select a sample frequency for time domain data, first divide the desired sample frequency by 2.56 to convert it to a measurement span. Then locate the closest measurement span on this table and choose the corresponding sample frequency at top of the table.

For a VT1432B which has the arbitrary source option, 1D4, the sample rate for the source is automatically set to be the same as the sample rate selected for the inputs. When the source is active, the sample rate cannot be greater than 65.536 kHz.

MEASUREMENT PROCESS

Measurement Setup and Control

When the VT1432B makes a measurement, the measurement itself consists of two phases: the measurement initialization and the measurement loop. Each of these phases consists of several states, through which the measurement progresses.

The transition from one state to the next is tied to a transition in the Sync/Trigger line (one of the TTL trigger lines on the VXI backplane.) A state (such as Idle) begins when the Sync/Trigger line goes low. The Sync/Trigger line then remains low as long as the state is in effect. When the Sync/Trigger line goes high, it signals the transition to the next state. See the *Measurement Initiation* and *Measurement Loop* sections below for more details about these transitions. During all the transitions of the Sync/Trigger line, the clock line continues with a constant pulse.

The Sync/Trigger line is "wire-OR'd" such that all modules in a multiple-module system (within one mainframe) must release it for it to go high. Only one VT1432B is required to pull the Sync/Trigger line low. In a system with only one VT1432B, the Sync/Trigger line is local to the module and not is routed to a TTL TRIGGER line on the VXI backplane.

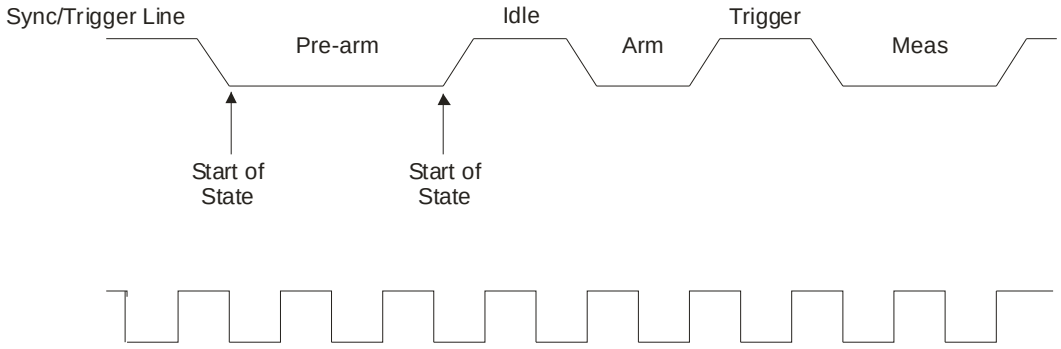


FIGURE 3-7: TRANSITIONS BETWEEN STATES

Parameter Settings

Many parameters are channel-dependent, meaning that each channel can be set independently of the others in the module. Other parameters are module-dependent; changing a module-dependent parameter for a channel will change it for all channels on that module. For example, changing blocksize, a module-dependent parameter, for input channel 3 will also change the block size for all other channels in the same VT1432B module as channel 3.

When possible, parameters are written to the hardware as soon as they are received. Sometimes, the parameter cannot be written to the hardware until the start of a measurement; in this case, the value of the parameter is saved in RAM in the VT1432B module until the measurement is started with vt1432_initMeasure. Some parameters can be changed while a measurement is running, but many do not take effect until the next start of a measurement.

Measurement Initiation

This section describes the measurement initiation process in the VT1432B.

The measurement initialization states and the corresponding sync/trigger line transitions (with 'H' for high, 'L' for Low) are:

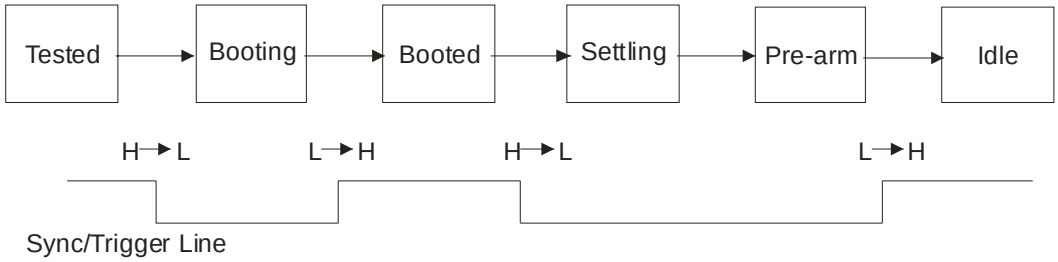


FIGURE 3-8: MEASUREMENT INITIALIZATION

The module enters the TESTED state after a reset. In this state, all of the module parameters may be set. The VT1432B stays in the TESTED state until it sees a high-to-low transition of the Sync/Trigger line.

In the BOOTING state, the digital processors of the module load their parameters and their program. Once done, the module releases the sync/trigger line and moves to the BOOTED state. The VT1432B stays in the BOOTED state until it sees a high-to-low transition of the Sync/Trigger line (that is, all the VT1432Bs in the system have booted).

In the SETTLING state, the digital filters are synchronized and the digital filter output is 'settled' (it waits *n* samples before outputting any data). Once the module is settled, it advances to the PRE_ARM state.

In the PRE-ARM state, the module waits for a pre-arm condition to take place. The default is to auto-arm, so the module would not wait at all in this case. When the pre-arm condition is met, the module releases the Sync/Trigger line and advances to the IDLE state.

This complete measurement sequence initialization, from TESTED through BOOTING, BOOTED, SETTLING, PRE-ARM, and IDLE, can be performed with a call to the function vt1432_initMeasure.

Measurement Loop

This section describes the measurement loop in the VT1432B.

The progression of measurement states and the corresponding sync/trigger line transitions are:

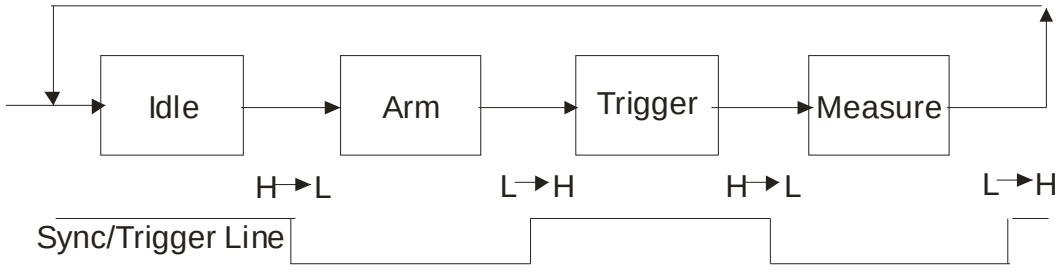


FIGURE 3-9: MEASUREMENT LOOP

In the IDLE state, the VT1432B writes no data into the FIFO. The VT1432B remains in the IDLE state until a high-to-low transition of the sync/trigger line occurs or an RPM arm/trigger point is calculated. If any of the VT1432Bs in the system are programmed for auto arming (with vt1432_setArmMode), the Sync/Trigger line is immediately pulled low by that VT1432B. The VT1432B may also be moved to the ARM state by an explicit call to the function vt1432_armMeasure.

Upon entering the ARM state, the VT1432B starts saving new data in its FIFO. It remains in the ARM state until the Sync/Trigger line goes high. If the VT1432B is programmed with a pre-trigger delay, it collects enough data samples to satisfy this pre-trigger delay and then releases the Sync/Trigger line. If no pre-trigger delay has been programmed, it releases the Sync/Trigger line immediately. When all modules in a system have released the Sync/Trigger line (allowing it to go high), a transition to the TRIGGER state occurs.

Upon entering the TRIGGER state, the VT1432B continues to collect data into the FIFO, discarding any data prior to the pre-trigger delay. The VT1432B remains in the TRIGGER state until it sees a high-to-low transition of the Sync/Trigger line. The Sync/Trigger line is pulled low by any VT1432B which encounters a trigger condition and is programmed to pull the Sync/Trigger line. If any VT1432B is programmed for auto triggering (with vt1432_setAutoTrigger), the Sync/Trigger line is pulled low immediately. The Sync/Trigger line may also be pulled low by an explicit call to the function vt1432_triggerMeasure.

Upon entering the MEASURE state, the VT1432B continues to collect data. The VT1432B also presents the first data from the FIFO to the selected output port, making it available to the controller to read. The VT1432B holds the Sync/Trigger line low as long as it is actively collecting data. In overlap block mode the VT1432B stops taking data as soon as a block of data has been collected, including any programmed pre- or post-trigger delays. (It starts again when another trigger occurs.) In continuous mode, the VT1432B stops taking data only when the FIFO overflows. When data collection stops, the VT1432B releases the Sync/Trigger line. When all VT1432Bs are finished and the Sync/Trigger line goes high, the VT1432B goes into the IDLE state again.

The measurement initialization and loop may be interrupted at any time with a call to vt1432_resetMeasure, which puts the module in the TESTED state.

Register-based VXI Devices

The VT1432B is a register-based VXI device. Unlike message-based devices which use higher-level programming using ASCII characters, register-based devices are programmed at a very low level using binary information. The greatest advantage of this is speed. Register-based devices communicate at the level of direct hardware manipulation and this can lead to much greater system throughput.

Users do not need to access the registers in order to use the VT1432B. The VT1432B's functions can be more easily accessed using the VT1432B VXI*plug&play* Library. However, more information about the registers is provided in *Appendix A*: *Register Definitions*.

Arm and Trigger

This section explains some terminology relating the "Arm" and "Trigger" steps in the measurement loop. As an example, a measurement might be set up to arm at a certain RPM level and then subsequently trigger at an external event corresponding to top dead center (TDC). The settings would be:

Arm:	RPM Step Arm
Trigger:	External Trigger

To begin a throughput session at this same RPM/TDC event, the first external trigger after a specified RPM should start a continuous mode measurement. Now (using overlap block mode), the settings would be:

Pre-Arm:	RPS Step Arm
Arm:	Auto
Trigger:	Auto

In the measurement loop, an arm must take place before a trigger. The number of triggers that occur before waiting for another arm condition can be defined. The default is one trigger for each arm. For each trigger, a block of data is sent to the host.

The first arm in a measurement is the pre-arm. By default, the pre-arm condition is the same as the regular arm conditions.

Valid Arm (and Pre-Arm) conditions are:

- Auto Arm
- Manual Arm
- RPM Step Arm

Valid trigger conditions are:

- Auto Trigger
- Input Trigger
- Source Trigger
- External Trigger
- Manual Trigger
- Tachometer Edge Trigger

Triggering

The following is a short discussion of triggering for the VT1432B.

Triggering is defined as the transition from the ARMED state to the TRIGGER state. This transition is caused by a low-going edge on a TTL trigger line. The function vt1432_getTtltrgLines selects which of the eight TTL trigger lines is to be used.

The low-going transition of the TTL trigger line can be caused by any of the following items:

Trigger Type	**Enabling Function**
the AUTO TRIGGER circuitry	vt1432_setAutoTrigger
the vt1432_triggerMeasure function	vt1432_triggerMeasure
a source trigger	vt1432_setTriggerChannel
a tach trigger	vt1432_setTriggerChannel
an external trigger	vt1432_setTriggerExt
an input level or bound trigger event	vt1432_setTriggerChannel and vt1432_setTriggerMode

Each of these trigger sources can be enabled or disabled independently, so quite complex trigger setups are possible. In all cases, however, the first trigger event kicks off the measurement and the following trigger events become superfluous.

Note that for vt1432_setAutoTrigger the setting VT1432_MANUAL_TRIGGER really means “do not auto trigger” not “expect a manual trigger.”

For single-VT1432B systems, the TTL trigger signal is not connected to the VXI backplane. For multiple VT1432B systems, the vt1432_initMeasure function connects the VT1432B trigger lines to the VXI backplane and at that point, the selection of which TTL trigger lines through

vt1432_getTtltrgLines is relevant. Multiple mainframe systems will need to account for the unidirectional nature of the inter-mainframe MXI extenders which will prevent all but the "upstream" mainframe from triggering the system.

Trigger Level

To set the trigger level, use vt1432_setTriggerMode to select "level" or "bound" mode; and use vt1432_setTriggerLevel twice to set both the upper and lower trigger levels. The difference between the upper and lower trigger levels must be at least 10% of full scale (and 10% is usually the best amount).

Also, use vt1432_setTriggerSlope to specify a positive or negative trigger slope.

Level mode

If the mode is set to "level" and the trigger slope is positive, then the module triggers when the signal crosses both the upper and lower trigger levels in the positive direction. If the trigger slope is negative, the module triggers when the signal crosses both levels in the negative direction. Setting two trigger levels prevents the module from triggering repeatedly when a noisy signal crosses the trigger level.

Bound mode

If the mode is set to "bound" and the trigger slope is positive, then the module triggers when the signal exits the zone between the upper and lower trigger levels in either direction. If the trigger slope is negative, the module triggers when the signal enters the zone between the upper and lower trigger levels.

Data Transfer Modes

The VT1432B can be programmed to use either of two data transfer modes: overlap block mode and continuous mode. Block mode will be described first.

Block Mode

In block mode, the input hardware acquires one block after getting an arm and trigger. It does not allow the system to trigger until it is ready to process the trigger and it acquires pre-trigger data if necessary. The hardware does not accept a new arm and trigger until the acquired block is sent to the host. There is no provision for overlap or queuing up more than one block when in block mode. There is also no way for a FIFO overflow to occur.

The VT1432B's overlap block mode can be configured to act exactly like traditional block mode. It also has additional capabilities as described below.

Continuous Mode

In this mode, the input hardware waits for an arm and trigger and then starts acquiring data continuously. If the host is slow, several blocks can be queued up in the input hardware. If the host gets far enough behind, a FIFO overflow occurs and the input stops acquiring data.

The VT1432B's overlap block mode can be configured to act similarly to continuous mode, but not identically. The VT1432B can also use the traditional continuous mode.

Overlap Block Mode

Overlap block mode combines features of both block mode and continuous mode. The main difference between overlap block mode and traditional block mode is that overlap block mode allows additional arms and triggers to occur before an already-acquired block is sent to the host. A trigger can occur before the end of the previous block, so overlapping blocks are possible (hence

the name “overlap block mode”). As in continuous mode, there is an overlap parameter which controls how much overlap is allowed between consecutive blocks.

Limit on Queuing of Data

In overlap block mode, a number of trigger events may be queued up before the host reads the data for those triggers. The host may get further and further behind the data acquisition.

However, if the host gets far enough behind that the FIFO fills-up, data acquisition must momentarily stop and wait for data to get transferred to the host. This places a limit on how far in time the host can be behind the data acquisition. By setting the size of the FIFO, it is possible to control how far behind the host can get.

Making Overlap Block Mode Act like Traditional Block Mode

If the FIFO size is set the same as the block size or if the number of pending triggers is limited to zero, then overlap block mode becomes identical to traditional block mode.

Making Overlap Block Act like Continuous Mode

If the module is in auto-arm and auto-trigger mode, then overlap block mode becomes nearly the same as continuous mode.

One difference is that traditional continuous mode has a single arm and trigger, while overlap block mode may have multiple arms and triggers. Another is that continuous mode can be configured to start at any type of trigger event, while overlap block mode must be in auto-trigger mode to act like continuous mode. Finally, continuous mode always stops when a FIFO overflow occurs, but overlap block mode does not.

INTERRUPT BEHAVIOR

Interrupt Setup

For an example of interrupt handling, see the program event.c in the examples directory.

The VT1432B VXI module can be programmed to interrupt a host computer using the VME interrupt lines. VME provides seven such lines. Using vt1432_setInterruptPriority, the VT1432B can be set up to use any one of them.

The VT1432B can interrupt the host computer in response to different events. Use vt1432_setInterruptMask to specify a mask of events on which to interrupt. This mask is created by OR'ing together the various conditions for an interrupt. The following table shows the conditions that can cause an interrupt:

Define (in vt1432.h)	Description
VT1432_IRQ_BLOCK_READY	Scan of data ready in FIFO
VT1432_IRQ_MEAS_ERROR	FIFO overflow
VT1432_IRQ_MEAS_STATE_CHANGE	Measurement state machine changed state
VT1432_IRQ_MEAS_WARNING	Measurement warning
VT1432_IRQ_OVERLOAD_CHANGE	Overload status changed
VT1432_IRQ_MEAS_STATE_CHANGE	Measurement state machine changed state
VT1432_IRQ_MEAS_WARNING	Measurement warning
VT1432_IRQ_OVERLOAD_CHANGE	Overload status changed
VT1432_IRQ_SRC_STATUS	Source channel interrupt
VT1432_IRQ_TACHS_AVAIL	Raw tachometer times ready for transfer to other modules
VT1432_IRQ_TRIGGER	Trigger ready for transfer to other modules

TABLE 3-2: INTERRUPT MASK BIT DEFINITIONS

Interrupt Handling

To make the VT1432B module cause an interrupt, both a mask and a VME Interrupt line must be specified by calling vt1432_setInterruptMask and vt1432_setInterruptPriority, respectively. Once the mask and line have been set and an interrupt occurs, the cause of the interrupt can be obtained by reading the VT1432_IRQ_STATUS_REG register (using vt1432_getInterruptReason). The bit positions of the interrupt mask and status registers match, so the defines can be used to set and check IRQ bits.

Once the interrupt occurs, the module will not cause any more VME interrupts until it is re-enabled using vt1432_reenableInterrupt. Normally, the last thing a host computer's interrupt handler should do is call vt1432_reenableInterrupt.

Events that would have caused an interrupt, but which are blocked because vt1432_reenableInterrupt has not yet been called, will be saved. After vt1432_reenableInterrupt is called, these saved events will cause an interrupt, so that there is no way for the host to "miss" an interrupt. However, the module will only do one VME interrupt for all of the saved events, so that the host computer will not get flooded with too many interrupts.

For things like "VT1432_IRQ_BLOCK_READY," which are not events, but, are actually states, the module will cause an interrupt after vt1432_reenableInterrupt is called only if the state is still present. This allows the host computer's interrupt handler to potentially read multiple scans from a VT1432B module and not get flooded with block ready interrupts after the fact.

Host Interrupt Setup

This is a summary of how to set up a VT1432B interrupt:

- Look at the Resource Manager to find out which VME interrupt lines are available.
- Tell the VT1432B module to use one of the VME interrupt line found in the step above, using the vt1432_setInterruptPriority call.
- Set up an interrupt handler routine, using the vt1432_callBackInstall call. The interrupt handler routine will be called when the interrupt occurs.
- Set up the interrupt mask in the VT1432B module, using the vt1432_setInterruptMask call.

Host Interrupt Handling

When the VT1432B asserts the VME interrupt line, the program will cause the specified interrupt handler to be called. Typically, the interrupt handler routine will read data from the module and then re-enable VT1432B interrupts with the vt1432_reenableInterrupt call. The call to vt1432_reenableInterrupt must be done unless the host is not interested in any more interrupts.

Inside the interrupt handler, almost any VT1432B Host Interface library function can be called. This works because the Host Interface library disables interrupts around critical sections of code, ensuring that communication with the VT1432B module stays consistent. Things that are not valid in the handler are:

- Calling vt1432_createChannelGroup to delete a group that is simultaneously being used by non-interrupt-handler code.
- Calling one of the read data functions (vt1432_readRawData or vt1432_readFloat64Data), if the non-interrupt-handler code is also calling one of these functions.
- Calling vt1432_init to reset the list of channels that are available to the VT1432B library.

As is always the case with interrupt handlers, it is easy to introduce bugs into the program and generally difficult to track them down. Be careful when writing this function.

Data Gating

Sometimes it is desirable to monitor data from some input channels and not from others. The function vt1432_setEnable enables or disables data from an input channel (or group of channels). If data is enabled, then the data can be read using the vt1432_blockAvailable and vt1432_readRawData call or the vt1432_readFloat64Data call. If data is disabled, data from the specified channel is not made available to the host computer.

This parameter can be changed while a measurement is running to allow the host computer to look at only some of the data being collected by the VT1432B module. While data from a channel is disabled, the input module continues to collect data, but it is not made available to the host computer. The host can then switch from looking at some channels to looking at others during the measurement. By contrast, the vt1432_setActive call completely enables or disables a channel and cannot be changed while a measurement is running.

For order tracking measurements, this function can be used to switch between receiving order tracking data, ordinary time data, or both.

Programming/Setup Parameters

Some parameters, such as range or coupling, apply to specific channels. When a channel ID is given to a function that sets a channel-specific parameter, only that channel is set to the new value.

Some parameters, such as clock frequency or data transfer mode, apply globally to a module. When a channel ID is used to change a parameter that applies to a whole module, the channel ID is used to determine which module. The parameter is then changed for that module.

Starting and stopping a measurement is somewhat like setting a global parameter. Starting a measurement starts each active channel in each module that has a channel in the group.

After firmware is installed and after a call to vt1432_preset is made, all of the parameters (both channel-specific and global) in the VT1432B module are set to their default values. For channel-specific parameters, the default value may depend on the type of channel. Some channel-specific parameters apply only to a specific type of channel. For example, tachometer holdoff applies only to tachometer channels. Setting a parameter for a channel that the parameter does not apply to will result in an error.

At the start of a measurement, the VT1432B firmware sets up all hardware parameters and ensures that the input hardware is settled before starting to take data. The firmware also ensures that any digital filters have time to settle. This ensures that all data read from the module will be valid.

However, after a measurement starts, VT1432B parameters can still be changed. The effect of this change varies, depending on the parameter. For some parameters, changing the value aborts the measurement immediately. For other parameters, the measurement is not aborted, but the changed parameter value is saved and not used until a new measurement is started. For still other parameters, the parameter change takes place immediately and the data coming from the module may contain glitches or other effects from changing the parameter. For more information, please see the *Programming Information* of the VT1432B VXI*plug&play* Library online help.

The module cannot be told to wait for settling when changing a parameter in the middle of a measurement. The only way to wait for settling is to stop and re-start the measurement. Also, the settling that takes place at the start of a measurement cannot be disabled.

Refer to the on-line VT1432B Function Reference for the parameters needed for each function. (See *Where to Get More Information* in this section.)

WHERE TO GET MORE INFORMATION

There is more information available about the VT1432B. This section shows how to access it and print it, if desired.

The Function Reference for VXIplug&play

On PCs, the VT1432B Functions Reference is provided in Microsoft Help text. Select the Help icon in the \<VXIPNP>\winNT\VT1432 directory. Refer to Windows documentation (including Help text) for information on using and printing Help.

SECTION 4

MODULE DESCRIPTION

UNIVERSAL MODULE FEATURES

The VT1432B 4-, 8-, and 16-channel 102.4 kSa/s digitizers plus DSP are VXI C-sized, scalable input modules. The VT1432B may contain up to four 4-channel input assemblies so that the module may have a total of up to 16 channels. The VT1432B-1DE is the 8-channel version of the VT1432B while the VT1432B-1DD has only 4 channels.

The VT1435 contains two 4-channel input assemblies for a total of 8 channels, and the VT1436 contains four 4-channel input assemblies making for 16 channels total. These modules also contain on-board IEPE current sources as well as the ability to read sensor's Transducer Electronic Data Sheets (TEDS) as described in the *Section 7*.

The following is a list of some of the features of the VT1432B, VT1435, and VT1436. See *Specifications* for more detailed information on the specific modules.

The standard VT1432B, as well as the voltage measurement sections of the VT1435/36, are described in this section. The arbitrary source and tachometer options are described in other sections. Features specific to the VT1435 and VT1436 are also discussed in this section.

General Features

- Fundamental sample rate selectable within the range of 40,960 Hz to 102,400 Hz.
- User-selectable digital sample rate decimation using FIR/IIR filtering in a 1, 2, 5 sequence.
- Variable block size (binary)
- Large data buffer (up to 16 MSa)
- Data from FIFO available with overlap
- VXI shared memory
- Flexible triggering, including pre- and post-triggering
- AC/DC coupling
- IEPE power supplies with the optional IEPE 8-channel input (via breakout box options)
- Overload detection
- Synchronous sampling over multiple channels and VT1432B modules
- Large FIFO for long pre-trigger delays
- D32 VME Bus data transfer
- VXI Local Bus data transfer (with Local Bus option)

In addition to the features mentioned above, the VT1435 and VT1436 have the following:

- Convenient SMB front panel connectors
- IEPE front panel transducer status LEDs
- On-board IEPE current source
- Transducer Electronic Data Sheet (TEDS) support (with the TEDS option)
- Single Ended Relay

Arbitrary Source Features (option 1D4)

- Sine output
- Random noise output
- Arbitrary output

Tachometer Features (option AYF)

- Current RPM value measurements
- Up/Down RPM triggered measurements

Other Options

- Local bus (UGV option)
- Transducer Electronic Data Sheet (TEDS, option , available on VT1435 and VT1436 only)

Block Diagram

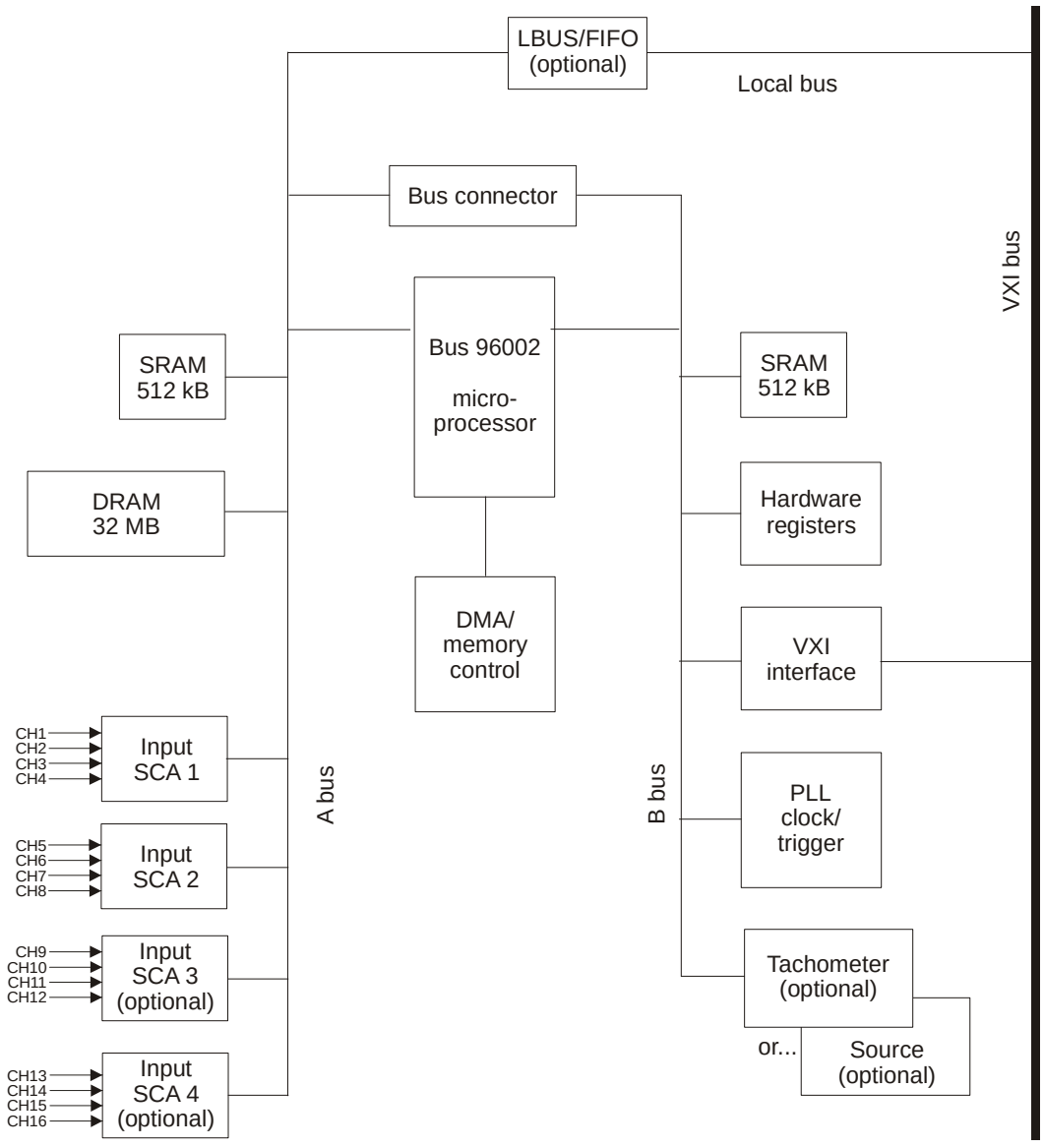


FIGURE 4-1: VT1432B BLOCK DIAGRAM

For block diagrams of the arbitrary source and the tachometer, see the sections on *The Arbitrary Source Option* and *The Tachometer Option*.

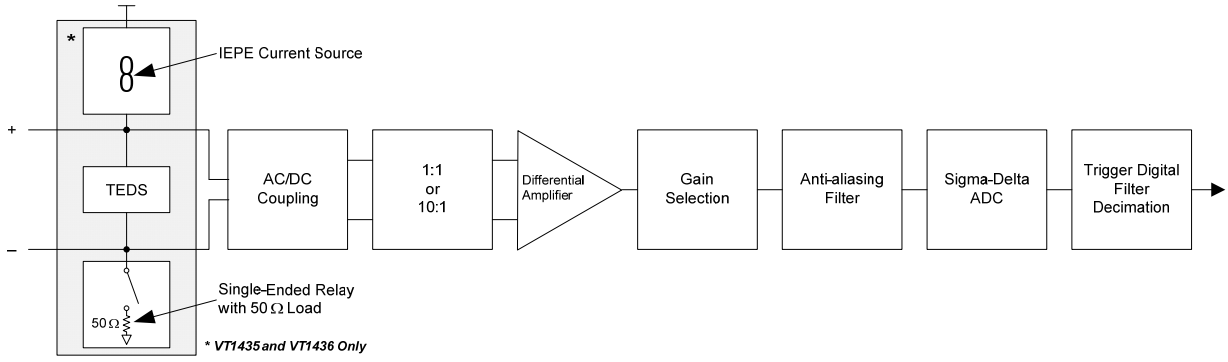


FIGURE 4-2: TYPICAL INPUT CHANNEL SECTION BLOCK DIAGRAM

VT1435 AND VT1436 SPECIFIC FEATURES

The following features are available only on the VT1435 and VT1436.

IEPE Current Source

The current source is set to a nominal 4 mA, and has a very high compliance voltage, and low output impedance. The current source is polarized, and must be operated with positive current flowing from the (+) terminal to the (-) terminal, and may not be operated in the opposite polarity. The voltage created by the current source's current flowing through and transducer is sampled internally, and directly controls the Status LED's state.

The IEPE function is enabled on a "by four" basis. The input connectors on the VT1435 are grouped onto two SCAs (signal conditioning assemblies), each four input connectors (channels 1 through 4 on one SCA and channels 5 through 8 on the other). The same is true for the VT1436, except four SCAs are used. If the IEPE current source is enabled on an SCA, all channels on the SCA will have their IEPE current source enabled. SCAs that do not have a current source enabled may be used for standard voltage measurements.

Each channel's current source is isolated, allowing operation of all channels in IEPE mode to float relative to one another. This is not the case when single-ended operation is selected.

Single-Ended Relay

The inputs of each channel are differential (+) and (-), but the VT1435/36 channels have the capability to connect the (-) terminal of each channel to system ground (GND). This feature makes each channel single-ended and, essentially, creates a non-isolated system by tying all channels (-) terminals to the same GND potential. The (-) terminals are connected to GND via a 50 Ω (nominal) positive temperature coefficient (PTC) resistor. If the module senses a channel's (-) terminal being forced to a potential other than GND via some external source, the 50 Ω resistor will increase and create a high resistance path from the (-) terminal to GND. This characteristic effectively creates an open circuit, disconnecting the (-) terminal from GND, safely allowing the channel to "float" to the potential to which it is being driven.

Transducer Electronic Data Sheet

Each channel of the VT1435/36 has the ability to *read* and *write* TEDS data from TEDS enabled transducers (DS2430A based devices only). For more information on the TEDS option, please see *Section 7*.

VT1432B FRONT PANEL DESCRIPTION

Front Panels for 4, 8, and 16 channels

The VT1432B may have any of several front panels depending on options and number of input channels. The following illustration shows front panels for 4, 8, and 16 channels.

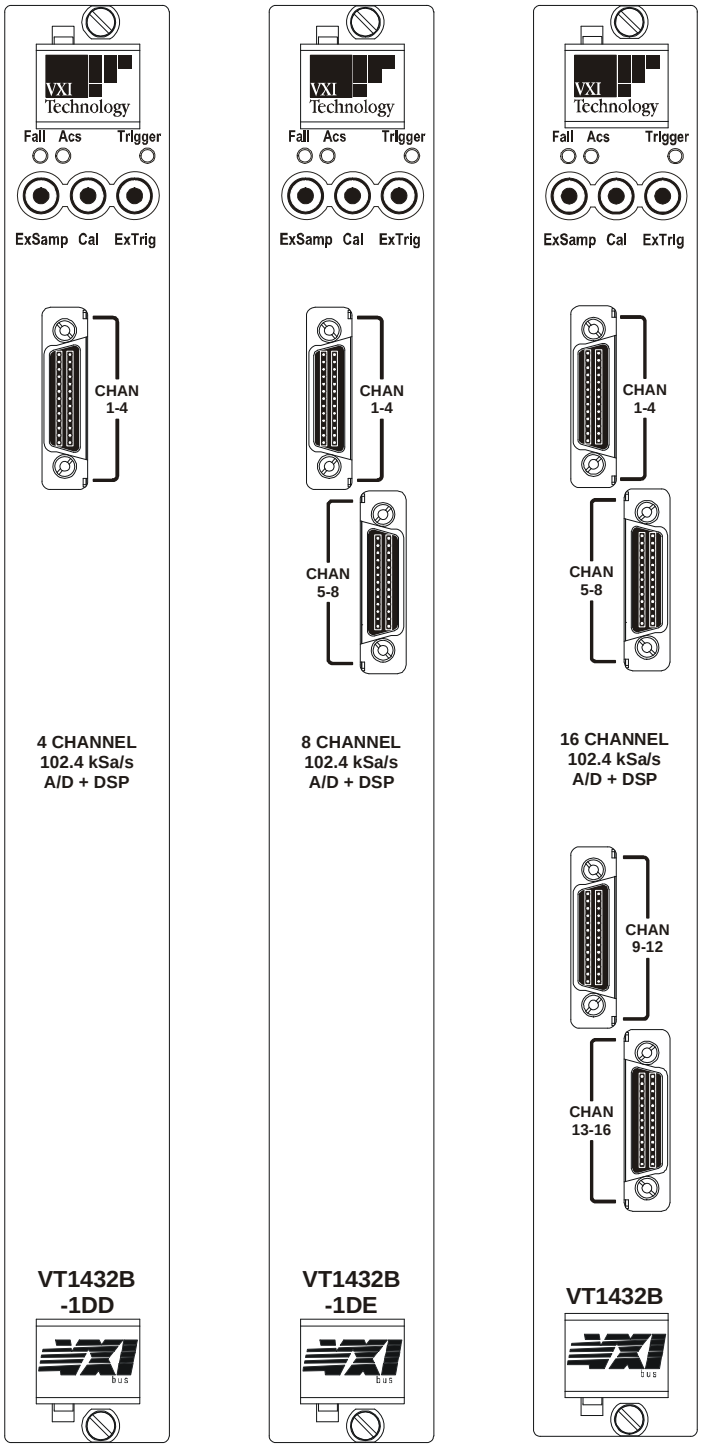


FIGURE 4-3: FRONT PANELS FOR 4, 8, AND 16 CHANNELS

Standard VT1432B Front Panel

This is the front panel for a standard VT1432B (this example has 16 inputs). The LEDs and connectors are described on the next page.

If the VT1432B has an arbitrary source (Option 1D4) or a tachometer (Option AYF), its front panel will be different. See *Section 5* and/or *Section 6* for a description the front panels for these options.

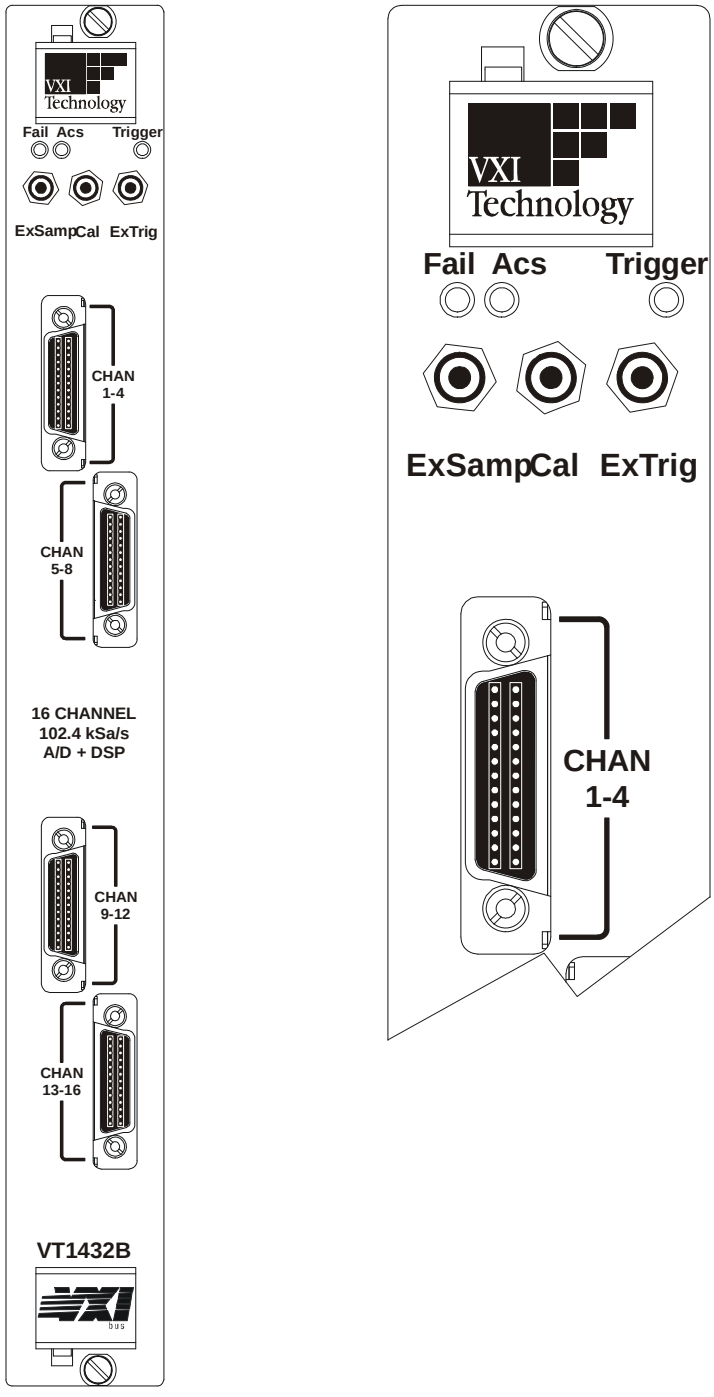


FIGURE 4-4: VT1432B STANDARD FRONT PANEL

Standard VT1435 and VT1436 Front Panels

The VT1435/36 may have any of several front panels depending on options and number of input channels. The following illustration shows front panels for 4, 8, and 16 channels.

If an arbitrary source (Option 1D4) or a tachometer (Option AYF) option is installed, its front panel will be different. See *Section 5* and/or *Section 6* for a description the front panels for these options.

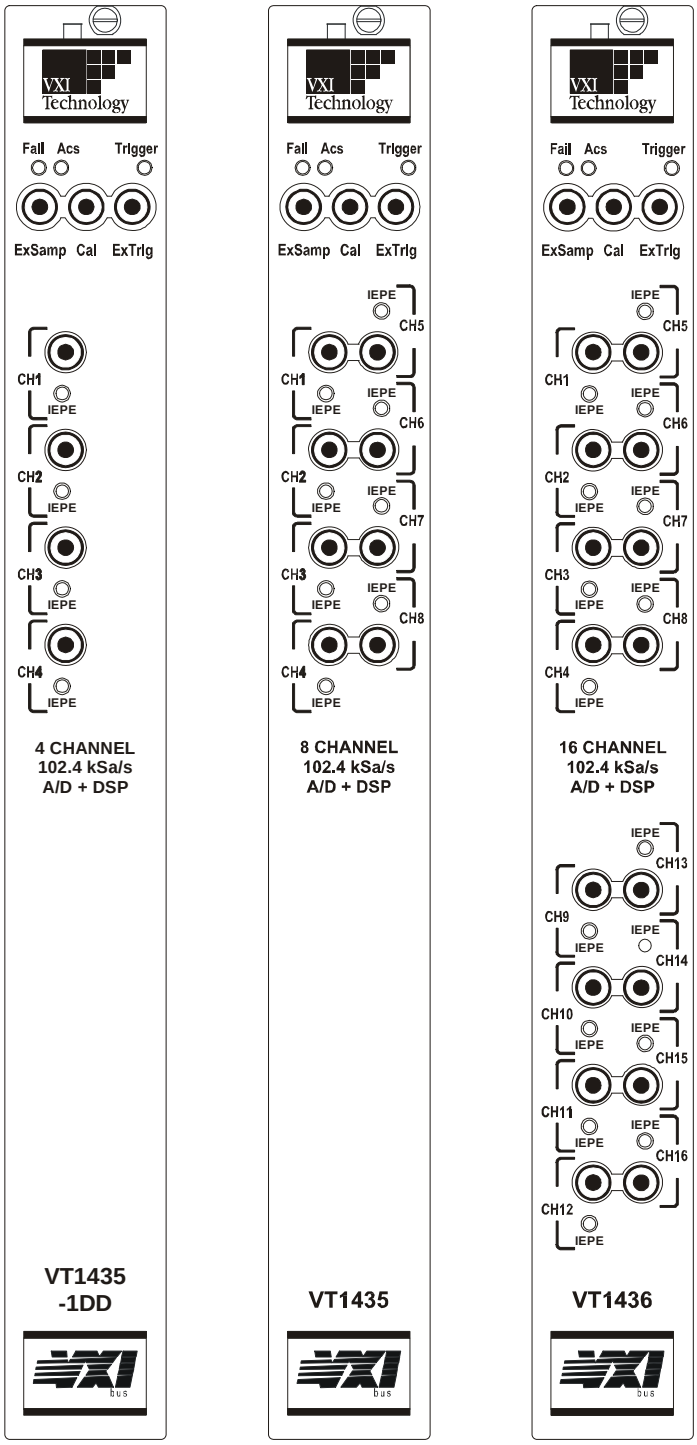


FIGURE 4-5: VT1435-1DD, VT1435, AND VT1436 FRONT PANELS

Status LEDs

- Fail: This is the standard VXI "Failed" indicator. It lights briefly when powering up and normally goes out after a few seconds. If it stays on, it indicates a hardware failure in the module.
- Acs: This is the standard VXI "Access" indicator. When it is on, it indicates that another device on the bus is contacting the module, for example, to transfer data or read registers.
- Trigger: This LED flashes on each time the measurement triggers, so when it is blinking it indicates that the measurement is triggering.

NOTE If the VT1432B has the tachometer option, the Trigger LED is defined differently. See *Section 6*.

- IEPE: (***VT1435 and VT1436 only***): This LED is associated with each input connector and displays the status of the IEPE transducer while the IEPE current source is enabled for the specified channel. If the IEPE current source is not enabled, then the LED will be non-illuminated. The operation of the LED is detailed below:

Condition	LED	Status
Transducer shorted	Illuminated – RED.	Short circuit detected
Transducer connected	Illuminated – GREEN.	Normal
Transducer not connected	Illuminated – RED	Open circuit detected.
IEPE Current Source turned OFF	Non-Illuminated	IEPE current source not enabled

SMB Connectors (not including channel input connectors)

- ExSamp: This is an input connector for an external sample clock. The sample clock must be TTL level and have a frequency between 40.96 kHz and 100 kHz. Internally, this frequency can be decimated.
- Cal: This connector is used for calibration. It can be configured to output a calibration signal or to accept an input calibration signal. See *Calibration Description* in this section.
- ExTrig: This allows for an external trigger input to the VT1432B. The input signal must be TTL, other characteristics can be defined in software. ExTrig can be enabled or disabled in software.

VT1432B Input Connectors

These connectors are attached to the cables from an 8-channel input (breakout box) — two input connectors for each 8-channel input. They connect the input signal to the VT1432B. Each connector carries four channels. Depending on options, there can be 2 or 4 input connectors (8 - 16 channels).

VT1435/VT1436 Input Connectors

These SMB input connectors connect the input signal to the VT1435/36 measurement circuitry. There are four SMB connectors per SCA measurement module. The VT1435 contains two SCAs and eight SMB connectors. The VT1436 contains four SCAs and sixteen SMB connectors. Each connector carries a single input channel. The center conductor of the SMB connector is the (+) input and the outer conductor of the SMB is the (-) input to the measurement circuitry. Each connector has an associated LED that displays the status of the IEPE transducer while the IEPE current source is enabled for the specified channel.

VXI BACKPLANE CONNECTIONS

Power Supplies and Ground

The VT1432B conform to the VME and VXI specifications for pin assignment. The current drawn from each supply is given in the respective specifications section.

Data Transfer Bus

The VT1432B conform to the VME and VXI specifications for pin assignment and protocol. A16, A24, D16, and D32 data transfers are supported.

DTB Arbitration Bus

The VT1432B module is not capable of requesting bus control. Thus, it does not use the Arbitration bus. To conform to the VME and VXI specifications, it passes the bus lines through.

Priority Interrupt Bus

The VT1432B generates interrupts by applying a programmable mask to its status bits. The priority of the interrupt is determined by the interrupt priority setting in the control register.

Utility Bus

The VME specification provides a set of lines collectively called the utility bus. Of these lines, the VT1432B only use the SYSRESET* line.

Pulling the SYSRESET* line low (a hardware reset) has the same effect as setting the reset bit in the Control Register (a software reset), except that pulling the SYSRESET* line low also resets the Control Register itself, while a software reset does not.

The Local Bus (UGV Option)

The VXI specification includes a 12-wire Local Bus between adjacent module slots. Using the local bus, a standard, byte-wide ECL protocol has been defined which can transfer data from left to right at up to 15.7 MB/s using the VT1432B. If equipped with the UGV option, the VT1432B can be programmed to output its data using this high-speed port instead of the VME data output register. The Data Port Control register determines which output port is used.

Local Bus vs. VME Transfers

With this option, data can be transferred from the VT1432B two different ways; via the VME Bus or via the local bus.

The VME Bus is the universal data bus for VXI architecture. It provides flexibility and versatility in transferring data. Transfers over the VME Bus can be 16 or 32 bits wide.

The Local Bus supports faster transfer rates than the VME Bus. For example, if data is transferred from the VT1432B to the VT2216A VXI/SCSI interface module, the local bus provides a direct pipeline to the VT2216A.

Using the local bus, data can be transferred in the background while processing data in a signal-processing module.

All Local Bus data transfers originate in an input module and move towards a signal processing or disk throughput module to the right of the input module. If other modules generate data to the left of the input module, the input module will pass the data to its right and append its own data to the data blocks from previous modules.

THE VT1432B VXI DEVICE

Address Space

The VXI system architecture defines two types of address space. A16 space consists of 64 kilobytes (kB) and A24 consists of 16 megabytes (MB).

The VT1432B have a 32-bit port through which it has access to the A16 and A24 space. It can also use D32 to send and receive data though the port. Or, it can use the port for 16-bit data transfers by using only 16 of the 32 bits available. The VT1432B perform different types of VME cycles depending on the number of bits transferred per cycle (two cycles for 16-bit transfers and one cycle for 32-bit).

Shared Memory

Shared memory provides a way for the VT1432B to transfer data to a controller. The shared memory in the VT1432B is mapped to the A24 VXI address space. The controller can then access that same address space to receive or write data. A function can be called to get the data.

Memory Map

The following discussion of memory mapping is included as supplemental information. It is not needed to operate the VT1432B as this functionality is hidden when using the VT1432B VXI*plug&play* Host Interface Library software.

Refer to the VT1432B (or VT1435/36) block diagram (Figure 4-1). The VXI interface maps some of the VT1432B's B-bus internal memory space so that it is visible to the VXI bus. The port connecting the A and B busses also allows the VXI bus access to the SRAM, DRAM, and inputs which are on the A bus. (SRAM stands for static RAM; DRAM is dynamic RAM.)

The VXI interface has two "windows" on the B bus memory space. Each is 512 kB, which is 128 32-bit words. One of the windows is fixed and the other is movable. The movable window allows the VXI bus access to many different parts of the memory space. The fixed window contains:

- The A16 registers
- The B-bus SRAM
- The hardware registers
- The FIFO (which is in DRAM)

The mapping of the fixed and movable windows is illustrated as follows:

Address		
F FFFF$_{16}$ 8 0000$_{16}$	Movable DSP Bus Window	Movable
7 FFFF$_{16}$ 3 0000$_{16}$	Fixed DSP Bus Window	Fixed
2 FFFF$_{16}$ 2 0000$_{16}$	Send/Receive Data Registers	
1 FFFF$_{16}$ 0 004F$_{16}$	Fixed DSP Bus Window	
0 003F$_{16}$ 0 0000$_{16}$	VXIbus A16 Registers	

For more information, see *The A24 Registers* in the section titled *Register Definitions*.

List of A16 Registers

The following lists the A16 registers. For more information, see *The A24 Registers* in the section titled *Register Definitions*.

Address	Read	Write
$3E_{16}$	Parameter 7 Register	
$3C_{16}$		
$3A_{16}$	Parameter 6 Register	
38_{16}		
36_{16}	Parameter 5 Register	
34_{16}		
32_{16}	Parameter 4 Register	
30_{16}		
$2E_{16}$	Parameter 3 Register	
$2C_{16}$		
$2A_{16}$	Parameter 2 Register	
28_{16}		
26_{16}	Parameter 1 Register	
24_{16}		
22_{16}	Query Response Register	Command Register
20_{16}		
$1E_{16}$	FIFO Count	
$1C_{16}$		
$1A_{16}$	Send Data	Receive Data
18_{16}		
16_{16}	RAM 1	
14_{16}		
12_{16}	RAM 0	
10_{16}		
$0E_{16}$	IRQ Status Register	IRQ Reset Register
$0C_{16}$	IRQ Config Register	
$0A_{16}$	Page Map Register	
08_{16}	Port Control Register	
06_{16}	Offset Register	
04_{16}	Status Register	Control Register
02_{16}	Device Type	
00_{16}	ID Register	Logical Address Register

Trigger Lines (TTLTRG)

TTLTRG consists of eight TTL lines on the VXI backplane on connector P2. They are available to provide synchronization between devices. VXI devices can use the TTLTRG lines for simple communication with other devices. For example, a device can wait for a line to go high before taking an action or it can assert a line as a signal to another device.

The VT1432B use two trigger lines. These can be placed on any two of the eight TTLTRG lines available on the VXI backplane. The lines are:

- Sync/Trigger line
- Free-running clock line

When programmed in a multiple-module configuration, only one of the VT1432B modules can provide the clock signal, but any of them can trigger.

Providing an External Clock

The VT1432B can be programmed to accept an external word rate clock from the sample 0 line on the VXI bus. The digital filters are still functional, providing a range of effective word rates. All sampling is done simultaneously and is not multiplexed.

To connect an external sample clock, use the External Sample SMB connector on front panel of the VT1432B. External sample at word rate and External Trigger are available on the front panel of VT1432B's that do not have an arbitrary source or tachometer option.

The external clock must be a fixed frequency. Its maximum frequency must not be higher than 100 kHz. Its minimum frequency must be at least 40.96 kHz.

CALIBRATION DESCRIPTION

The Cal connector on the front panel of the standard VT1432B can be configured (in software) as either an input or an output. It can be set to any of four settings:

- DC - the VT1432B outputs a dc calibration signal from the millivolt range up to 15 V.
- AC - the VT1432B outputs a signal from an arbitrary source option (in the same module or a different VT1432B module in the system).
- Ground - the connector is shunted to ground for a 0 V reference.
- Open Circuit - in this mode, the connector becomes an input which can receive a calibration signal up to ±15 V.

The VT1432B is calibrated at the factory and the calibration placed in EPROM memory for use at each power-up. In addition, an auto-zero function is provided.

SECTION 5

THE ARBITRARY SOURCE OPTION (1D4)

ARBITRARY SOURCE DESCRIPTION

An arbitrary source can be included with the VT1432B, VT1435, and VT1436 digitizers as Option 1D4. (It cannot be installed with a tachometer, Option AYF). The arbitrary source option can supply arbitrary or sine signals under control of measurement software.

Trigger

The arbitrary source can be used to trigger the measurement and to trigger other modules in the measurement system.

Arbitrary Output

The arbitrary source can be programmed to output any signal that is described by data downloaded by the software.

Source Output Modes

The arbitrary source has several output modes including the following:

- arbitrary
- sine
- noise
- random
- burst

COLA (and Summer)

The COLA (Constant Output Level Amplifier) output supplies a signal similar to the source “Out” output except that it is at a constant output level of about one volt peak.

The same connector (labeled “COLA”) can also be programmed as a summer input. A signal connected to this input is summed with the internal source output to create the final output.

External Shutdown

Shorting the center pin of the shutdown connector to its shield causes the source to ramp down and shut off.

Block Diagram

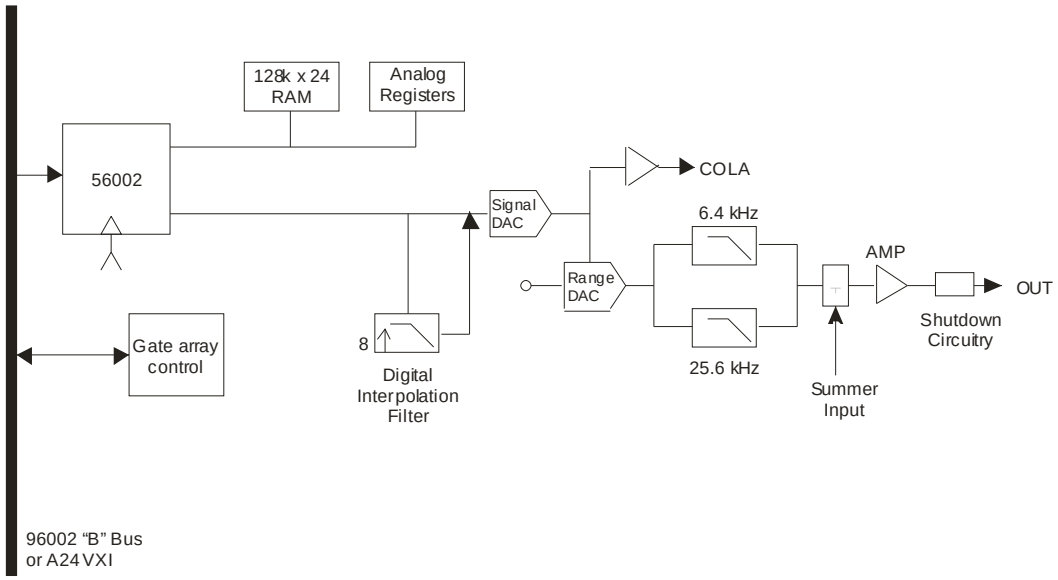


FIGURE 5-1: SOURCE OPTION BLOCK DIAGRAM

THE ARBITRARY SOURCE OPTION FRONT PANEL

The VT1432B with the arbitrary source option may have 8 or 16 input channels. The following illustration shows a front panel for 16-channels (VT1432B), as well as the front panels for the VT1435 and VT1436 with tachometer option. The LEDs and connectors are described on the next page and function identically for either the VT1432B or VT1435/36 modules.

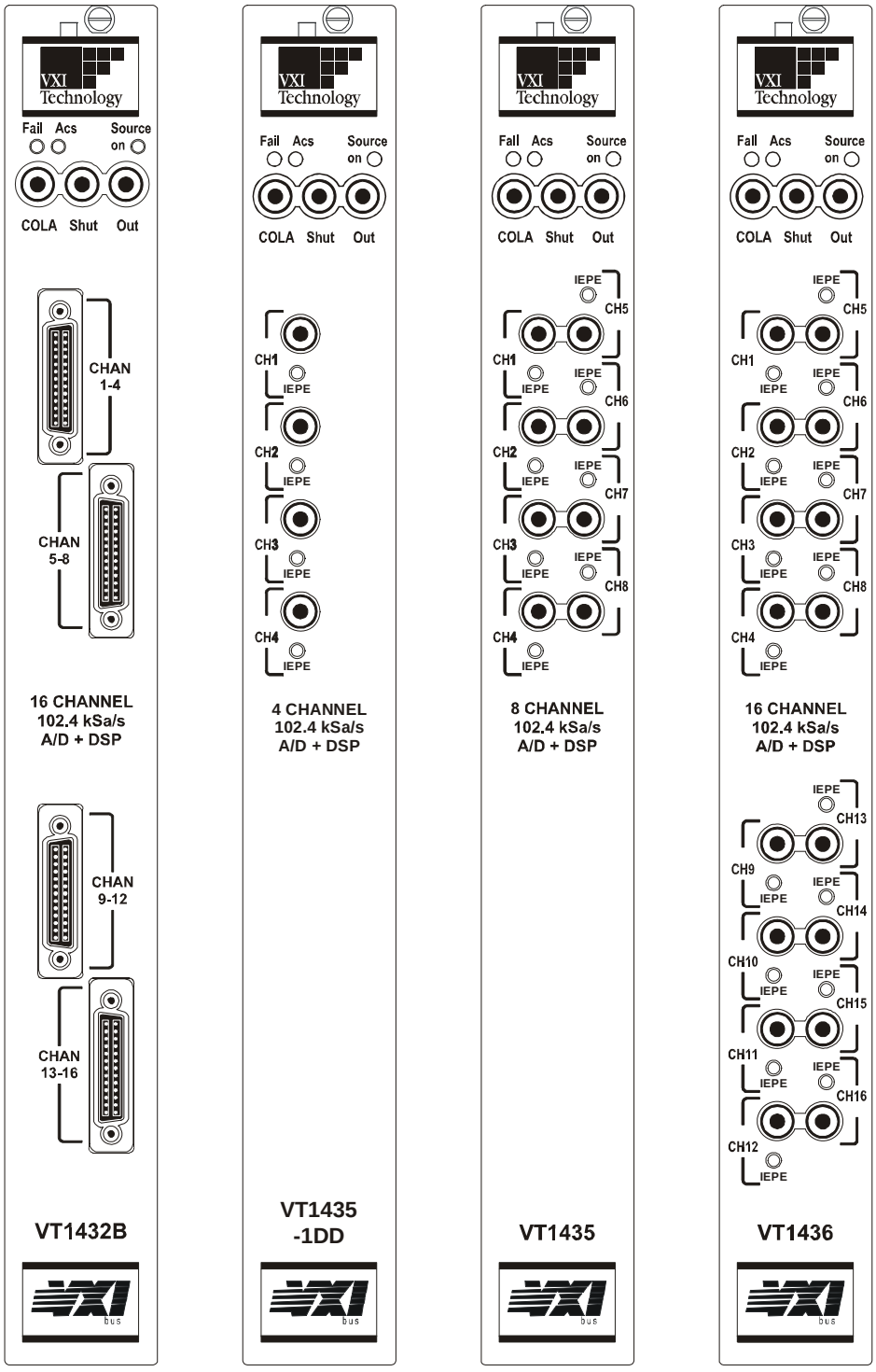


FIGURE 5-2: ARBITRARY SOURCE OPTION FRONT PANELS

LEDs and Connectors for the Arbitrary Source Option

Status LEDs

- Fail: This is the standard VXI "Failed" indicator. It lights briefly when powering up and normally goes out after a few seconds. If it stays on, it indicates a hardware failure in the module.
- Acs: This is the standard VXI "Access" indicator. When it is on, it indicates that another device on the bus is contacting the module, for example to transfer data or read registers.
- Source: If this LED is illuminated, it indicates that the source is on and producing output.
- IEPE: (***VT1435 and VT1436 only***): This LED is associated with each input connector and displays the status of the IEPE transducer while the IEPE current source is enabled for the specified channel. If the IEPE current source is not enabled, then the LED will be non-illuminated.

SMB Connectors (not including channel input connectors)

- COLA: This is the output connector for the COLA (Constant Output Level Amplifier) output. This connector can also be configured as a summer input. A signal connected to this input is summed with the internal source output to create the final output.
- Shut (Shutdown): Shorting the center pin of this connector to its shield causes the source to ramp down and shut off.
- Out: This is the main output of the arbitrary source.
  The Out connector can also be configured to output a calibration signal. This is not quite the same as the calibration signal described in *Section 4* because it comes directly from the internal source without going through the other circuitry of the calibration section.

VT1432BInput Connectors

These connectors are attached to the cables from an 8-channel Input (breakout box.) There are two input connectors for each 8-channel Input. They connect the input signal to the VT1432B. Each connector carries four channels. Depending on options, there can be 2 or 4 input connectors (8 - 16 channels.)

VT1435/VT1436 Input Connectors

These SMB input connectors connect the input signal to the VT1435/36 measurement circuitry. There are four SMB connectors per SCA measurement module. The VT1435 contains two SCAs and eight SMB connectors. The VT1436 contains four SCAs and sixteen SMB connectors. Each connector carries a single input channel. The center conductor of the SMB connector is the (+) input and the outer conductor of the SMB is the (-) input to the measurement circuitry. Each connector has an associated LED that displays the status of the IEPE transducer while the IEPE current source is enabled for the specified channel.

Updating the arbitrary source firmware

When updated firmware for the arbitrary source is available, the ROM in the VT1432B can be updated by using the procedure documented in \<VXIPNP>\winNT\VT1432\source\read.me.

SECTION 6

THE TACHOMETER OPTION (AYF)

TACHOMETER DESCRIPTION

Option AYF provides two tachometer inputs. When this option is installed, two of the three SMB connectors on the VXI module are used for tachometer inputs. When this option is not installed, these connectors are normally used for "External Sample" and "Trigger." Each tachometer input has a programmable trigger level. Each tachometer pulse causes a "Tach Edge Time" to be recorded in a 16 kword FIFO. A "Tach Edge Time" is the instantaneous value of the 32-bit "Tach Counter". A "Decimate" number can be set to ignore a number of tachometer pulses before recording each Tach Edge Time. A "Holdoff" time can be set to avoid false triggering due to ringing.

One of the tachometer inputs can be programmed for use as a trigger input rather than a tachometer input. In this mode, the tachometer option can trigger the system and measure the time between the trigger and the next sample clock edge. The analog signal from either of the tachometer inputs can be routed to an input channel using the internal calibration path.

Tachometer Inputs

The tachometer has two inputs that connect to analog conditioning, holdoff, and FIFO circuitry. See the Figure 6-1. The inputs can be configured so that one input connector (Tach 2) becomes an external trigger input and the other (Tach 1) remains a tachometer input. (The Tach 1 connector cannot be a trigger input.) The switch that determines this configuration is controlled by software.

External Trigger Input

A VT1432B without a tachometer option can accept a TTL external trigger signal (see *Trigger Lines (TTLTRG)* in *Section 4*). With the tachometer option, the VT1432B retains this capability and is also able to accept an analog external trigger signal at the Tach 2 input.

Trigger Level

The trigger level of the tachometer can be set by software.

Tachometer Monitoring

The tachometer is capable of sending its analog input signal onto the VT1432B module's internal calibration line. The calibration line can be connected to the 102.4 kHz 4-channel input assembly, so that the signal on the tachometer's connector can be monitored via an input channel. This can be useful when deciding where to set the trigger level of the tachometer. An example program is supplied with the VT1432B host interface library, which shows how to perform this tachometer monitoring.

Exact RPM Triggering

The tachometer can be used to create exact rpm triggering, controlled by software. The rpm of the tachometer channel is calculated from tachometer transition times. Then, the sample numbers in the data FIFO are determined for exact rpm triggering.

Input Count Division

The tachometer can be programmed to divide the input signal. For example, if a signal is coming in at 100 counts per second, the tachometer can be set to look at only every 10^{th} count for a result of 10 counts per second.

Holdoff Time

The tachometer can be programmed to wait for a specified period of time between counts that it will detect. After a count is detected, subsequent counts will be ignored until the holdoff time has passed.

Block Diagram

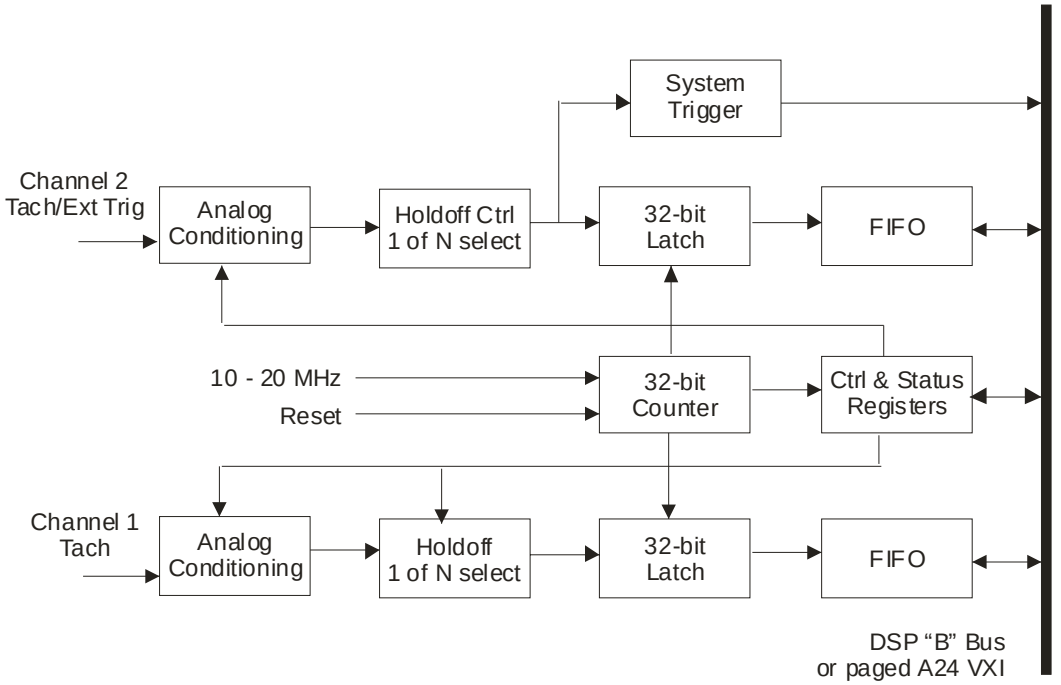


FIGURE 6-1: TACHOMETER OPTION BLOCK DIAGRAM

THE TACHOMETER OPTION FRONT PANEL

The VT1432B with the tachometer option may have 8 or 16 input channels. The following illustration shows a front panel for a 16-channel VT1432B, as well as the front panels for the VT1435 and VT1436 with tachometer option. The LEDs and connectors are described on the next page and function identically for either the VT1432B or VT1435/36 modules.

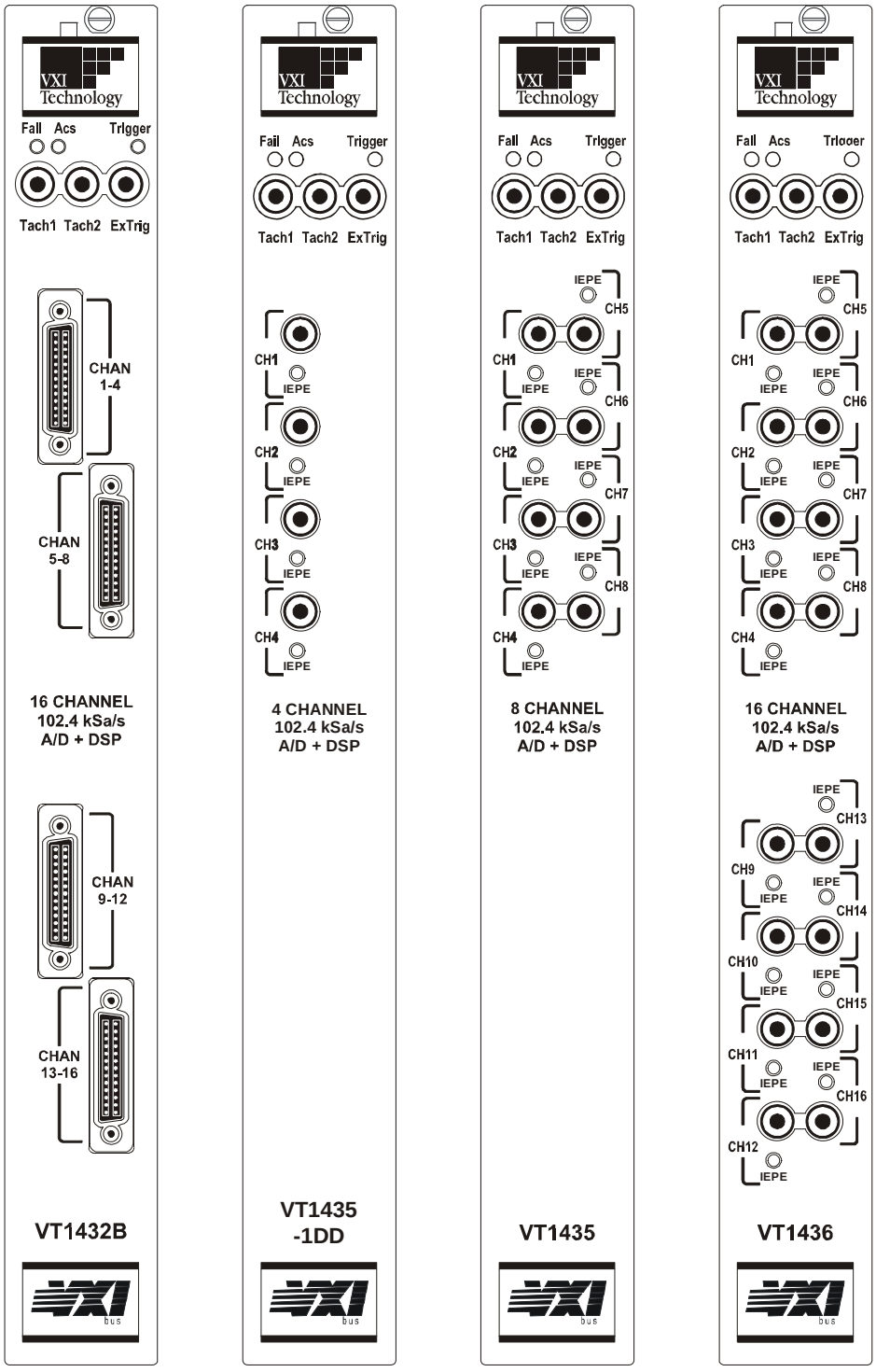


FIGURE 6-2: TACHOMETER OPTION FRONT PANELS

LEDs and Connectors for the Tachometer Option

Status LEDs

- Fail: This is the standard VXI "Failed" indicator. It lights briefly when powering up and normally goes out after a few seconds. If it stays on, it indicates a hardware failure in the module.
- Acs: This is the standard VXI "Access" indicator. When it is on, it indicates that another device on the bus is contacting the module, for example to transfer data or read registers.
- Trigger: This LED flashes on each time an edge is detected on the tachometer signal, so when it is blinking, it indicates that the tachometer signal is on. (For a VT1432B that does not have the tachometer option, this LED is defined differently.)
- IEPE: (***VT1435 and VT1436 only***): This LED is associated with each input connector and displays the status of the IEPE transducer while the IEPE current source is enabled for the specified channel. If the IEPE current source is not enabled, then the LED will be non-illuminated.

SMB Connectors (not including channel input connectors)

- Tach1: This is one of the two tachometer inputs. Tach1 cannot be configured as an external trigger.
- Tach2: This is the second of the two tachometer inputs. Tach2 can also be configured (via software) to be an external trigger input.
- ExTrig: This allows for an external trigger input to the VT1432B. The input signal must be TTL, although other characteristics can be defined in software. ExTrig can be enabled or disabled in software.

VT1432BInput Connectors

These connectors are attached to the cables from an 8-channel Input (breakout box) – two input connectors for each 8-channel Input.) They connect the input signal to the VT1432B. Each connector carries four channels. Depending on options, there can be 2 or 4 input connectors (8 - 16-channels).

VT1435/VT1436 Input Connectors

These SMB input connectors connect the input signal to the VT1435/36 measurement circuitry. There are four SMB connectors per SCA measurement module. The VT1435 contains two SCAs and eight SMB connectors. The VT1436 contains four SCAs and sixteen SMB connectors. Each connector carries a single input channel. The center conductor of the SMB connector is the (+) input and the outer conductor of the SMB is the (-) input to the measurement circuitry. Each connector has an associated LED that displays the status of the IEPE transducer while the IEPE current source is enabled for the specified channel.

SECTION 7

THE TEDS OPTION (TEDS)

TRANSDUCER ELECTRONIC DATA SHEET (VT1435 AND VT1436 ONLY)

Each channel of the VT1435/36 has the ability to *read* and *write* TEDS data from TEDS enabled transducers (DS2430A based devices only). In *read* mode, the module will return the device's *8-bit family code, 48-bit serial number, 8-bit CRC, and 32-byte user calibration data fields.* There is no processing on the VT1435/36 to format the data read from the TEDS device.

In *write* mode, the module expects 40 bytes of data. The first 8 bytes are ignored and take the place of the family code, serial number, and CRC bytes. The last 32 bytes are destined for the TEDS device's 32-byte EEPROM. It is recommended that the user first *read* the contents of the TEDS device (40 bytes), change the user modifiable EEPROM 32 bytes as required, and then *write* the new values to the device. Note: When writing to the 32-byte EEPROM, all 32 bytes must be written to at the same time.

The vt1432_writeTEDS function contains many data verification steps to assure that *write* data is correctly written to the TEDS device. If data is correctly written to the device, the function call returns no error. It should be noted that the write function of a TEDS device has many exacting timing constraints, and interruption by the user of this function could result in lost data or corrupted EEPROM memory. Care should be taken in both the hardware setup of the transducer and associated cabling, and the software routines controlling the write function during this phase of operation of the TEDS device.

For information on upgrading the VT1435/36 or replacing parts, contact VXI Technology Customer Support Services. See the *Support Resources* section in the preface of this manual for contact information.

NOTES

As the TEDS option is a firmware upgrade, there is no hardware upgrade necessary for this option to be installed. It can be installed at the factory at the time of original hardware purchase, or purchased at a later date and upgraded in the field at the customer's site.

Once this option is installed, the TEDS operation as described above is enabled and available for use on all channels of the VT1435 or VT1436 module for which it was purchased. For proper operation, each VT1435/36 module that requires TEDS functionality must have this option installed.

TEDS FIELD UPGRADE

To perform a field upgrade of a VT1435/6 to enable the TEDS option, the following procedure can be used:

1) Contact VXI Technology Customer Support Services and provide the serial number of the VT1435/6. The serial number is typically found on the outside of the VT1435/6 module on a label.
2) VXI Technology Customer Support Services will supply a "TEDS Code Word" that will be used to enable the TEDS feature on the module.

3) Set the module's address to 0x8.
4) Install the module to be upgraded into a VXI chassis and turn the power on.
5) Run Resman or and equivalent program.
6) Open a Command Line window by navigating to Start→Run→Cmd.
7) In the Command Line window, navigate to the directory that contains the Option Loading Program (OLP).

NOTE	**The OLP is installed during the VT1432 driver installation. If the driver has not been installed, this should be done at this step. The OLP is typically located at C:\progam files\visa\ winnt\vt1432\bin or other appropriate location on the host hard drive.**

Example:

```
Cd\ <rtn>
Cd\ progam files\visa\winnt\vt1432\bin <rtn>
```

8) Run the OLP "progopt.exe" program.

Example:

```
progopt –h
```

Usage:

```
progopt [-RuVZ] [-A optStr] [-D optStr] [-L laddr]
```

Read or Write E1432 PARM2 block
-A: Add option optstr to option list
-D: Delete option optstr from option list
-L: Talk to logical address <laddr>, default 8
-R: Read option list from hardware
-S: Read serial string from hardware
-u: Print this usage message
-V: Print version info
-Z: Zero (delete) all options from option list

Example:

```
progopt –A "TEDS Code Word"
```
(as supplied by VTI Customer Service)

9) Verify that the "TEDS Code Word" has been accepted by the module.

Example:

```
progopt –R

option0 "CodeWord"
```

NOTE	The module may have other options already installed, and the new TEDS option may not necessarily be option0.

10) Connect a TEDS capable device to the module and verify correct TEDS operation.

SECTION 8

BREAKOUT BOXES (VT3240A AND VT3241A)

INTRODUCTION

A breakout box connects the VT1432B or VT1433B to a set of connectors to receive input signals. Note that breakout boxes are not required for the VT1435/36 modules, as the IEPE current sources are built-in on-board the modules and may be enabled via software control.

Several types of breakout boxes are available. This section covers:

- VT3240A Voltage Breakout Box
- VT3241A IEPE Breakout Box

Other breakout boxes include the VT3242A charge breakout box and the VT3243A microphone breakout box. See the documentation supplied with those products for more information.

Service

For service on the breakout boxes, contact the nearest VXI Technology Customer Support center.

THE VT3240A AND VT3241A BREAKOUT BOXES

Each of the breakout boxes described in this section has eight BNC connectors for input. They each have two cables that connect to the sub-miniature "D" connectors on the front panel of the VT1432B. Each of the two cables carries four channels. For a 16-channel VT1432B, two breakout boxes are used.

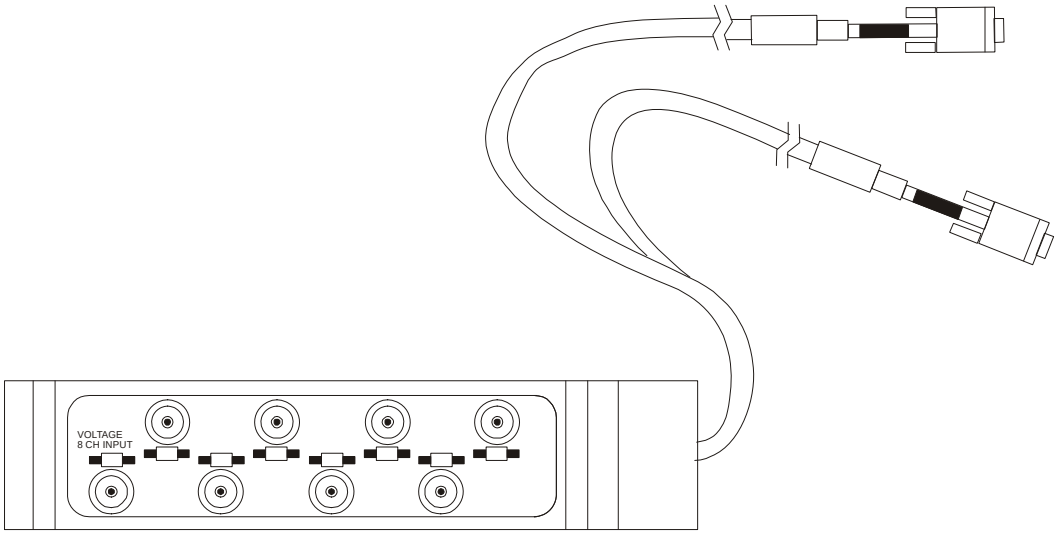


FIGURE 8-1: VT3240A VOLTAGE BREAKOUT BOX

VT3240A Voltage-type Breakout Box

In this type of breakout box, the signal is sent straight through to the sub-miniature "D" connectors on the VT1432B.

VT3241A IEPE/Voltage Breakout Box

Each of the eight connectors in this type of breakout box is connected to an independent, floating current source. These are intended to power integrated electronics piezoelectric (IEPE) transducers. They supply 4.5 mA (nominal) at up to 28 V. The current sources are controllable by software in groups of four. That is, the current sources for connectors 1-4 can be turned on or off as a group as can the current sources for connectors 5-8.

Breakout Box Grounding

Each connector on the VT3240A and VT3241A breakout box has a small manual switch next to it. When this switch is in the "GND" position the outer shell of the connector is grounded to the chassis ground of the VXI mainframe. When it is in the "DIFF" position, it is not grounded to the mainframe and will float if not grounded elsewhere in the system (such as at the sensor). The connector shell should not be allowed to float: if the switch is in the "DIFF" position, the shell should be grounded elsewhere in the system.

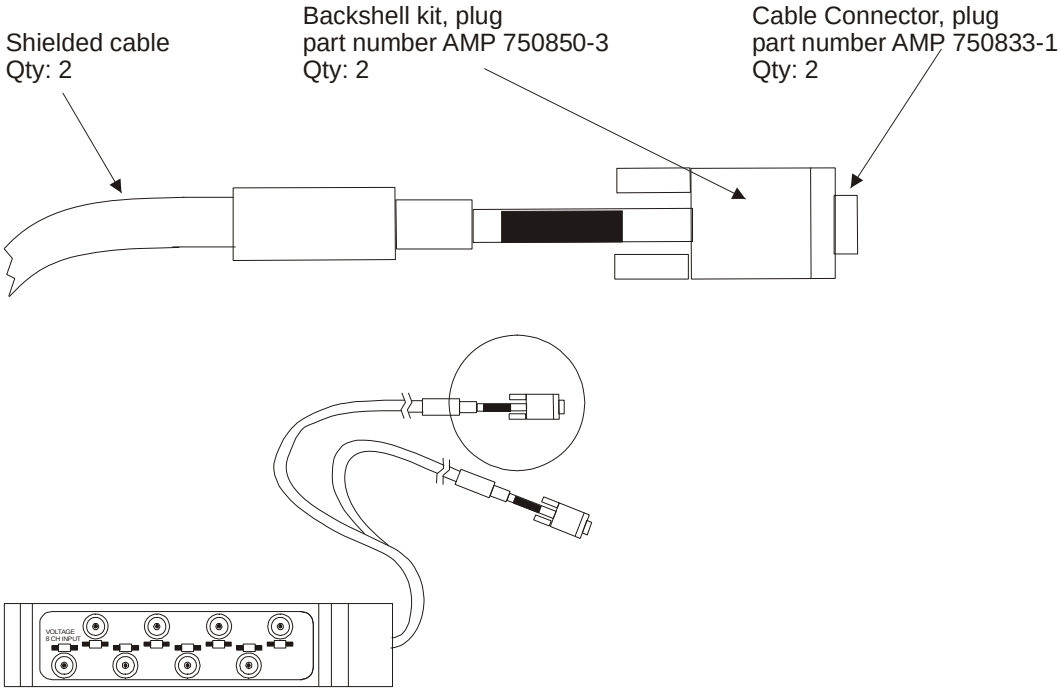


FIGURE 8-2: BREAKOUT BOX CABLE AND PART NUMBERS

BREAKOUT BOX CABLES

Making a Custom Breakout Box Cable

A cable to connect the breakout box with the VT1432B is supplied with the each of the breakout boxes described in this section. However, this section is included for those users who may want to make their own connecting cable. Figure 8-2 shows the AMP part numbers for the parts needed to make the plug end of the cable. This illustration shows a VT3240A voltage breakout box; a VT3242A breakout box requires a single cable with connectors at both ends.

The next page shows the pinout for the connector.

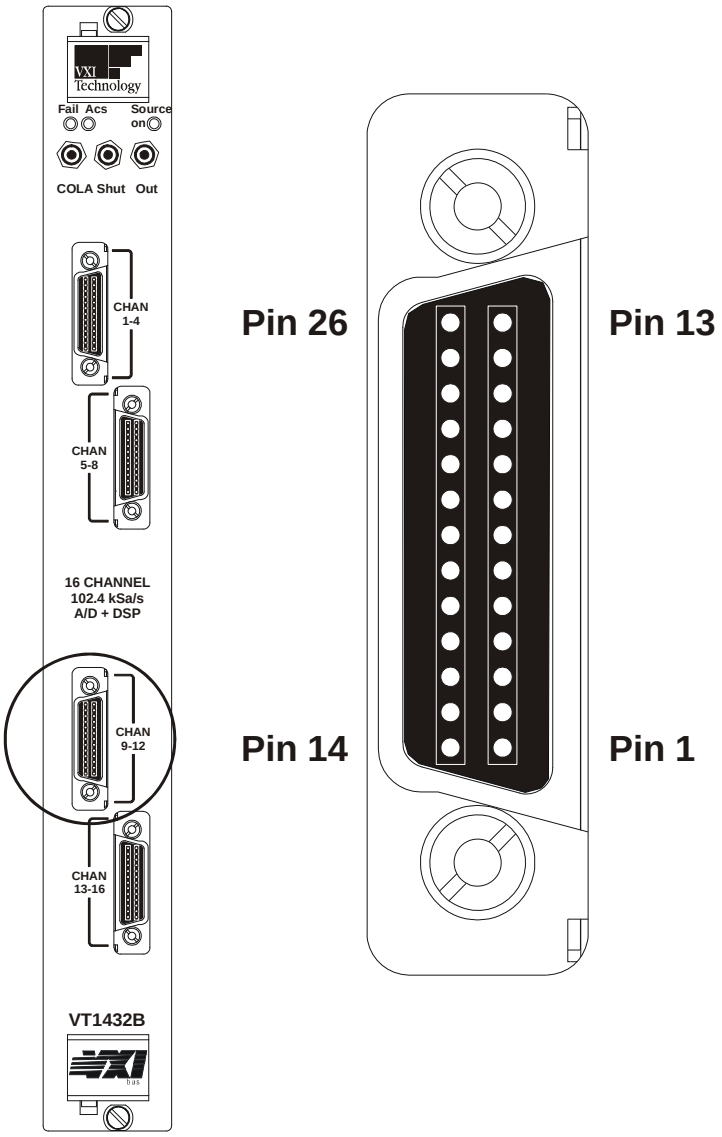


FIGURE 8-3: VT1432B CONNECTOR PIN LOCATIONS

Definition	Pin #		Pin #	Definition
RFI GND/Cable Shield	26		13	- Diff 1
+24 V Power	25		12	+Diff 1
GND Return for ±24 V	24		11	RFI GND/Drain Shield 1
-24 Power	23		10	RFI GND/Drain Shield 2
RFI GND	22		9	- Diff 2
I2C SCL	21		8	+ Diff 2
CAL HIGH	20		7	CAL LOW
BoB_EN	19		6	- Diff 3
RFI GND	18		5	+ Diff 3
I2C SDA	17		4	RFI GND/Drain Shield 3
RFI GND	16		3	RFI GND/Drain Shield 4
I2C_EN	15		2	- Diff 4
RFI GND/Cable Shield	14		1	+ Diff 4

TABLE 8-1: PIN DEFINITIONS FOR INPUT CONNECTOR

Recommendations on wiring for the VT1432B 4-channel Input Connector

Allowed Connections

Differential Input Channels Connect at VT1432B end of cabling and at DUT Recommended: shielded twisted pair	
1	+ Diff 4
2	- Diff 4
5	+ Diff 3
6	- Diff 3
8	+ Diff 2
9	- Diff 2
12	+ Diff 1
13	- Diff 1

Input Channel Shielding Connect at VT1432B end of cabling ONLY	
3	RFI GND/Drain Shield 4
4	RFI GND/Drain Shield 3
10	RFI GND/Drain shield 2
11	RFI GND/Drain Shield 1

Additional shielding of entire cable GND for grounded measurements if required	
14	RFI GND/Cable Shield
26	RFI GND/Cable Shield

Disallowed Connections

Do NOT connect these pins on VT1432B end of cabling. These signals and supplies are provided for VXI Technology specified breakout boxes and are unspecified for other usage.

Do not use:	
15	I2C_EN
17	I2C_SDA
21	I2C_SCL
16	RFI GND/I2C Shield
18	RFI GND/I2C Shield
22	RFI GND/I2C Shield
19	BOB_EN
7	CAL_LOW
20	CAL_HIGH
23	±24 V Power
24	±24 V GND Return
25	+24 V Power

In general:

- ± DIFF n lines are the differential inputs for each channel. Shielded twisted pair is recommended.
- RFI GND/Drain Shield n are the grounds for the shield on the twisted pair for each input channel. Connect at the VT1432B end of the cable only.
- RFI GND/Cable Shield are the grounds for a shield around the entire cable and the ground points for making individual channels single-ended.
- I2C_xxx supply control signals to the active breakout boxes. Support for other usage is not provided. These are not used with the VT3240/1A Voltage and Voltage/IEPE breakout boxes.
- RFI GND/I2C Shield protects the analog input lines.
- BOB_EN is another breakout box control signal. Support for the usage of these breakout boxes is restricted to those that are VXI Technology-specified.
- CAL_HIGH/LOW are signal lines to send calibration signals to VXI Technology-specified breakout boxes. The signals available on these lines are not specified and their usage is discouraged.
- ±24 V Power and GND supply power to the signal conditioning circuitry in the active breakout boxes and IEPE in the active IEPE breakout box. The power available on these lines is not specified and their usage is discouraged.

SECTION 9

TROUBLESHOOTING THE VT1432B

DIAGNOSTICS

The following describes a limited diagnostic program for the VT1432B, VT1433B, VT1434A, VT1435, and VT1436. The program is called "hostdiag.exe." It can be found with the VT1432B Host Interface Software Library at location \<VXIPNP>\winNT\VT1432\bin.

Usage: hostdiag [-hPsuvV] [-f file] [-L laddr] [-S slot] [-O list]

-h
Does a quick, partial test by bypassing the tests which involve downloading code to the module.

-f file
Uses "file" as the source of code to download to the module instead of the default sema.bin.

-L logical_addr
Specifies the logical address of the module to be tested. The default value is 8.

-O option_list
Tests the module against a list where the model and options are defined. For example, -O "VT1432,1DE,VT1432B-AYF" tests the module as an 8-channel VT1432B with the tachometer option. Without this option, hostdiag only tests what it finds present. Hardware which has failed in such a way that it appears to be absent will not be detected without this option.

-P
Prints only a pass/fail message - no diagnostic printouts.

-s
Runs the "standard input/output" tests in addition to the other diagnostic tests. Sources finish testing with 1 V peak, 1 kHz sine on each output for manual verification of output functionality. Input testing (both VT1432B and VT1433B inputs and the Tachometer input) assumes 1 V peak, 1 kHz sine input on each channel. This allows testing of additional portions of the signal path which are inaccessible from the internal tests.

-S vxi_slot
Tests the module in the vxi slot, vxi_slot. The default is to test the module at logical address 8.

-u
Display usage message.

-v
Specifies the verbose printing. Normally, hostdiag does not print anything unless an error is found. With this option, hostdiag prints status messages as it operates. This option also enables additional diagnostic information which is not generally useful.

-V
Print version info.

Hostdiag returns 0 upon success or returns non-zero if an error is detected.

Coverage:

Main board

- DRAM SIMMs
- Input SCAs (Signal Conditioning Assemblies)
- Source SCAs (VT1434A)
- Optional source
- Optional tachometer (VT1432B/35/36 and VT1433B)

Notes

- Tests are somewhat limited but will catch many hardware errors
- No errors printed means that all tests passed

SECTION 10

REPLACING ASSEMBLIES

REPLACEABLE PARTS

For information on upgrading the VT1432B or replacing parts, contact VXI Technology Customer Support Services. See the *Support Resources* section in the preface of this manual for contact information.

Replacement parts are listed in the following tables:

- Assemblies: without option AYF or 1D4
- Assemblies: with option AYF
- Assemblies: with option 1D4
- Assemblies: with option TEDS (VT1435/36 only, see VT1435/36 Section)
- Cables: without option AYF or 1D4
- Cables: with option AYF
- Cables: with option 1D4
- Front Panel

Ordering Information

To order a part listed in one of the tables, quote the part number (VTI Part Number), indicate the quantity required, and address the order to the nearest VXI Technology sales and service office (see the preface of this manual). The first time a part is listed in the table, the quantity column (Qty) lists the total quantity of the part used in the module. For the corresponding name and address of the manufacturer's codes shown in the tables, see *CAGE Code Numbers*.

CAUTION	The module is static sensitive. Use the appropriate precautions when removing, handling, and installing to avoid unnecessary damage.

Direct Mail Order System

Within the U.S.A., VXI Technology can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

- Direct ordering and shipment from VXI Technology.
- No maximum or minimum on any mail order.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.
- Mail order forms and specific ordering information are available through VXI Technology. See *Support Resources* for a list of VXI Technology sales and service office locations and phone numbers.

CAGE Code Numbers

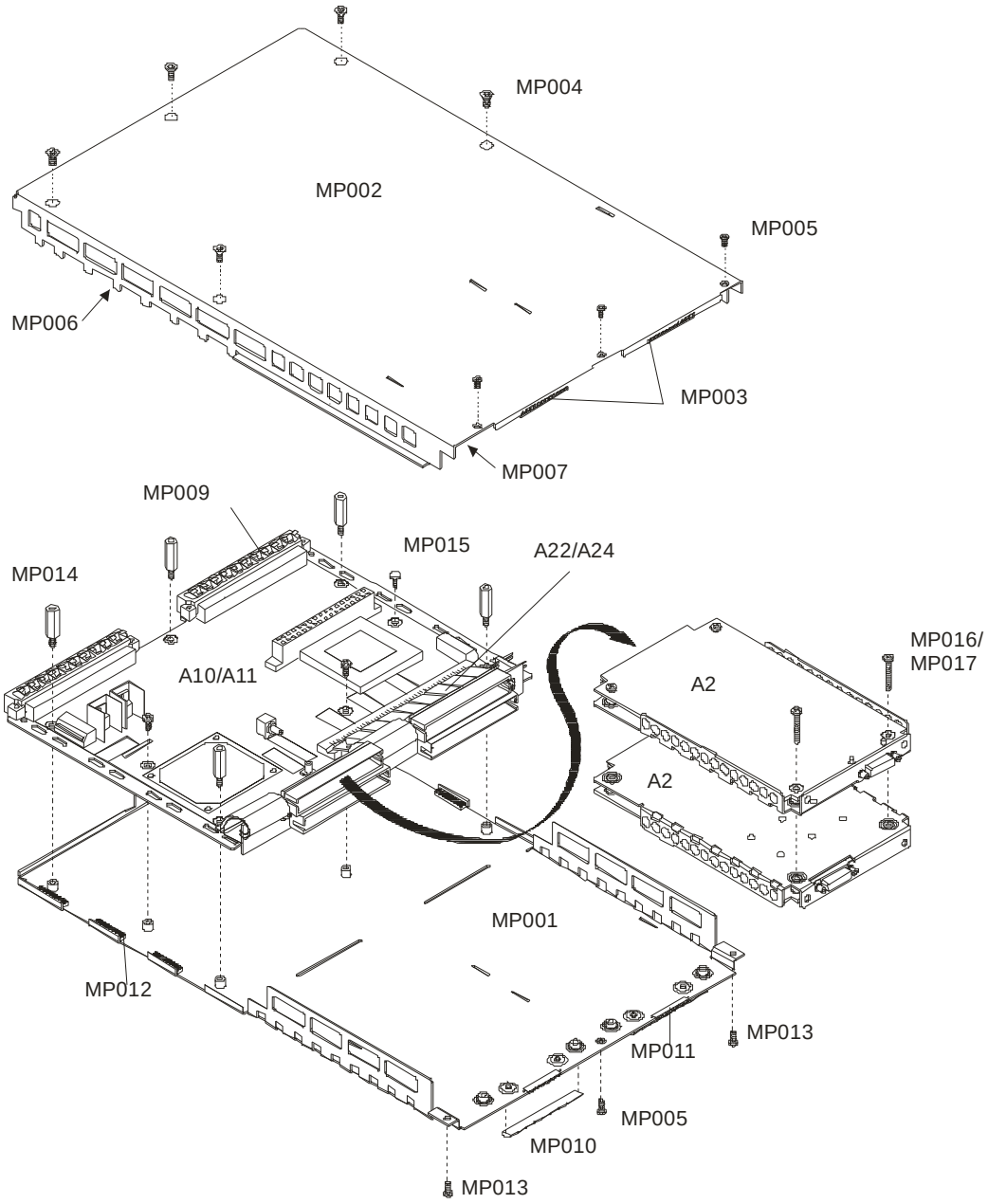
The following table provides the name and address for the manufacturers' CAGE (Commercial And Government Entity) code numbers (Mfr Code) listed in the replaceable parts tables.

Mfr Code	Mfr Name	Address
0PL50	Quantum Graphics, Inc.	Redmond, WA 98052 U.S.A.
03LB1	VXI Technology, Inc.	Irvine, CA 92614 U.S.A.
05791	Lyn-Tron, Inc.	Spokane, WA 99224 U.S.A.
30817	Laird Technologies	Delaware Water Gap, PA 18327 U.S.A.
77824	Schlegel Systems, Inc.	Rochester, NY 14623 U.S.A.
93907	Textron Fastening Systems	Decorah, IA 52101 U.S.A.

The manufacturer's listed below have not requested CAGE code numbers. The Mfg Code provided is arbitrarily assigned and used for purposes of identification in this user's manual only.

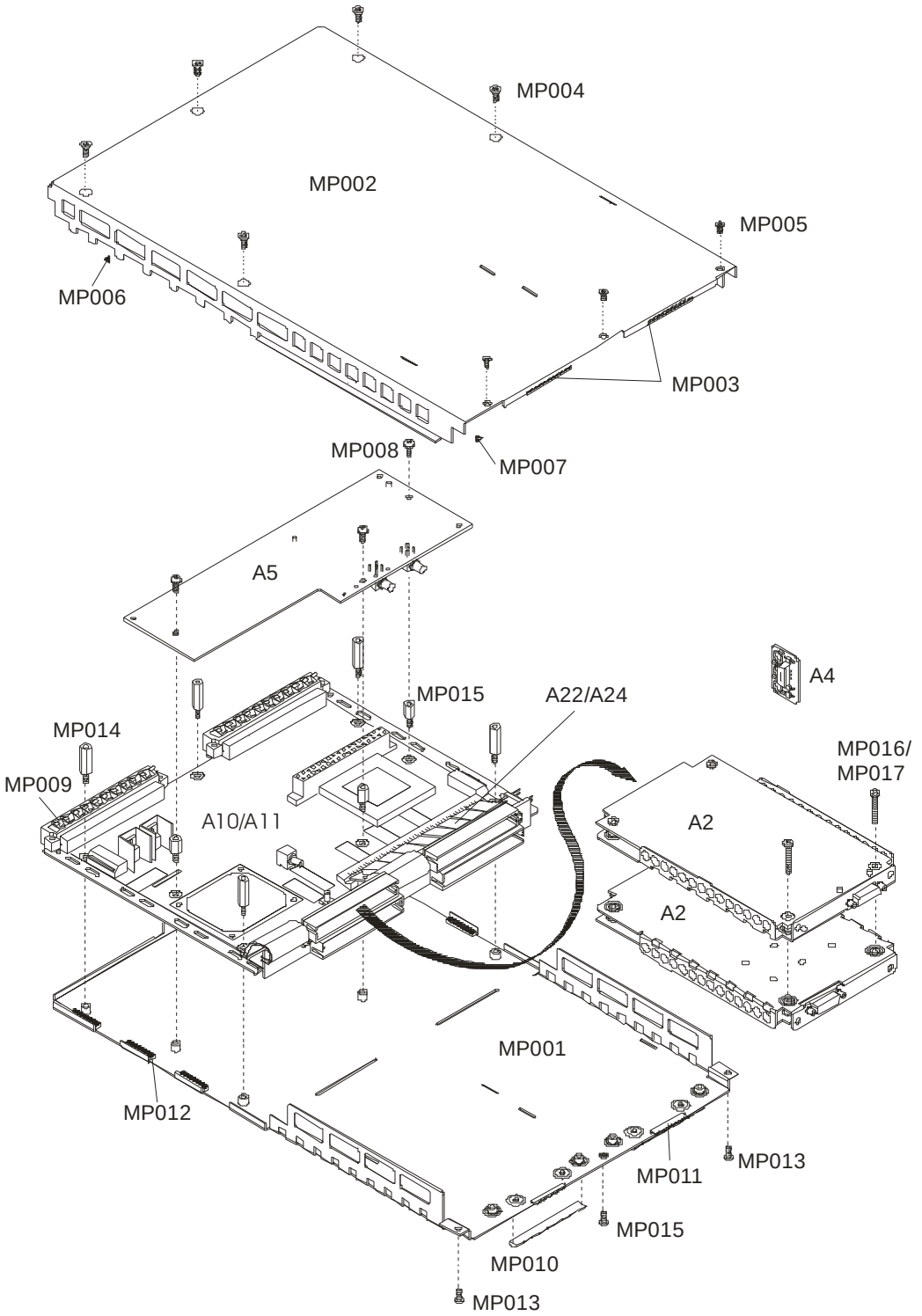
Mfr Code	Mfr Name	Address
N046	Boyd Corporation	Modesto, CA 95357 U.S.A.
N091	Illinois Tool Works, Inc.	Tempe, AZ 85281 U.S.A.
N109	Laird Technologies	Littleton, CO 80120 U.S.A.
N114	Littlefuse, Inc.	Denver, CO 80222 U.S.A.
N116	Logan Industries, Inc.	Spokane, WA 99216 U.S.A.
N118	Mason Cable& Assembly, Inc.	Enumclaw, WA 98022 U.S.A.

Assemblies: without Option AYF or 1D4



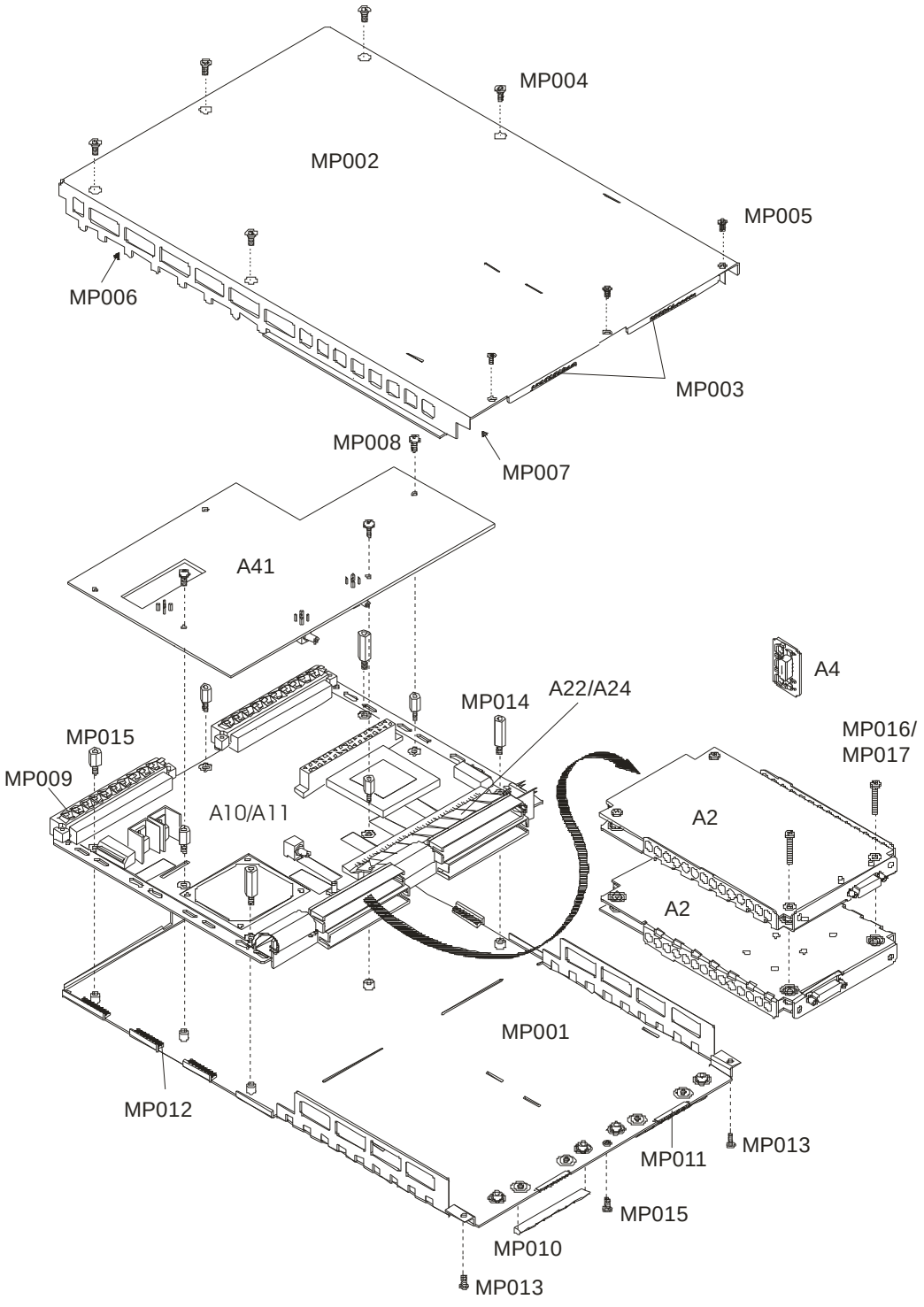
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2	52-0459-000	4	VT1432B PC ASSY-INPUT	03LB1	52-0459-000
A2	52-0560-000	4	VT1435 PC ASSY-INPUT	03LB1	52-0560-000
A4	E1432-66504	1	PC ASSY-LED	66049	E1432-66504
A10	E1433-66910	1	PC ASSY-MAIN OPT -UGV	03LB1	E1433-66510
A11	E1433-66911	1	PC ASSY-MAIN	03LB1	E1433-66511
A22	1818-5622	1	ICM DRAM, SIMM, 8x32	N121	MT16D832M-6
A24	1818-5624	1	ICM DRAM, SIMM, 1x32	N90	HYM532100AM-70
MP001	41-0403-000	1	SHTF CVR-BTTM ALSK	03LB1	41-0403-000
MP002	41-0402-000	1	SHTF CVR-TOP	03LB1	41-0402-000
MP003	8160-0862	2	GSKT RFI STRIP FNGRS	N109	0786-318
MP004	0515-2033	5	SCR-MCH M3.0 10MMLG	N091	0515-2033
MP005	0515-2028	4	SCR-MCH M2.5 6MMLG	N091	0515-2028
MP006	E1432-44101	1	GSKT THERMAL CONDUCTOR	N046	E1432-44101
MP007	E1485-40601	1	GSKT-RFT, TOP CVR ADH SHT	77824	5774-194W-0
MP008	0515-0372	3	SCR-MCH M3.0 8MMLG	93907	0515-0372
MP009	8160-0634	4	STMP SHLD-RFI GRND	N109	8160-0634
MP010	8160-0686	1	STMP FNGRS-RFI STRP BECU	N109	786-185
MP011	8160-0683	1	STMP STRP-SPNG FLTR GRD	N109	0097-551-17-X
MP012	8160-0869	6	GSKT RFI, 2MM X 4MM	77824	E8119T00090
MP013	0515-0368	2	SCR-MCH M2.5 X 0.45	N091	0515-0368
MP014	0380-4042	5	STDF-HXMF M3.0 16.7MMLG	05791	SS5172-16.7-01
MP016	0515-2383	2/4	SCR-MCH M3.0 12MMLG	03LB1	0515-2383

Assemblies: with Option AYF



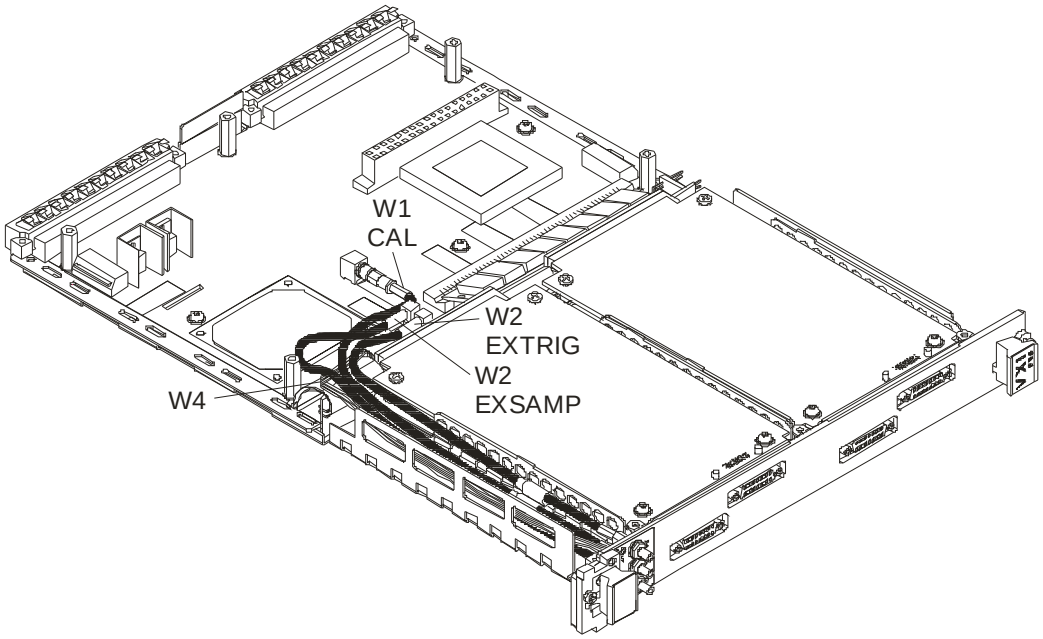
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2	52-0459-000	4	VT1432B PC ASSY-INPUT	03LB1	52-0459-000
A2	52-0560-000	4	VT1435 PC ASSY-INPUT	03LB1	52-0560-000
A4	E1432-66504	1	PC ASSY-LED	66049	E1432-66504
A5	E1432-66505	1	PC ASSY-OPT -AYF	03LB1	E1432-66505
A10	E1433-66910	1	PC ASSY-MAIN OPT -UGV	03LB1	E1433-66510
A11	E1433-66911	1	PC ASSY-MAIN	03LB1	E1433-66511
A22	1818-5622	1	ICM DRAM, SIMM, 8x32	N121	1818-5622
A24	1818-5624	1	ICM DRAM, SIMM, 1x32	N90	HYM532100AM-70
MP001	41-0403-000	1	SHTF CVR-BTTM ALSK	03LB1	41-0403-000
MP002	41-0402-000	1	SHTF CVR-TOP	03LB1	41-0402-000
MP003	8160-0862	2	GSKT RFI STRIP FNGRS	N109	0786-318
MP004	0515-2033	5	SCR-MCH M3.0 10MMLG	N091	0515-2033
MP005	0515-2028	4	SCR-MCH M2.5 6MMLG	N091	0515-2028
MP006	E1432-44101	1	GSKT THERMAL CONDUCTOR	N046	E1432-44101
MP007	E1485-40601	1	GSKT-RFT, TOP CVR ADH SHT	77824	5774-194W-0
MP008	0515-0372	3	SCR-MCH M3.0 8MMLG	93907	0515-0372
MP009	8160-0634	4	STMP SHLD-RFI GRND	N109	8160-0634
MP010	8160-0686	1	STMP FNGRS-RFI STRP BECU	N109	786-185
MP011	8160-0683	1	STMP STRP-SPNG FLTR GRD	N109	0097-551-17-X
MP012	8160-0869	6	GSKT RFI, 2MM X 4MM	77824	E8119T00090
MP013	0515-0368	2	SCR-MCH M2.5 X 0.45	N091	0515-0368
MP014	0380-4042	5	STDF-HXMF M3.0 16.7MMLG	05791	SS5172-16.7-01
MP015	0380-4041	3	STDF-HXMF M3.0	05791	SS5172-15.0-01
MP016	0515-2383	2/4	SCR-MCH M3.0 12MMLG	N091	0515-2383

Assemblies: with Option 1D4



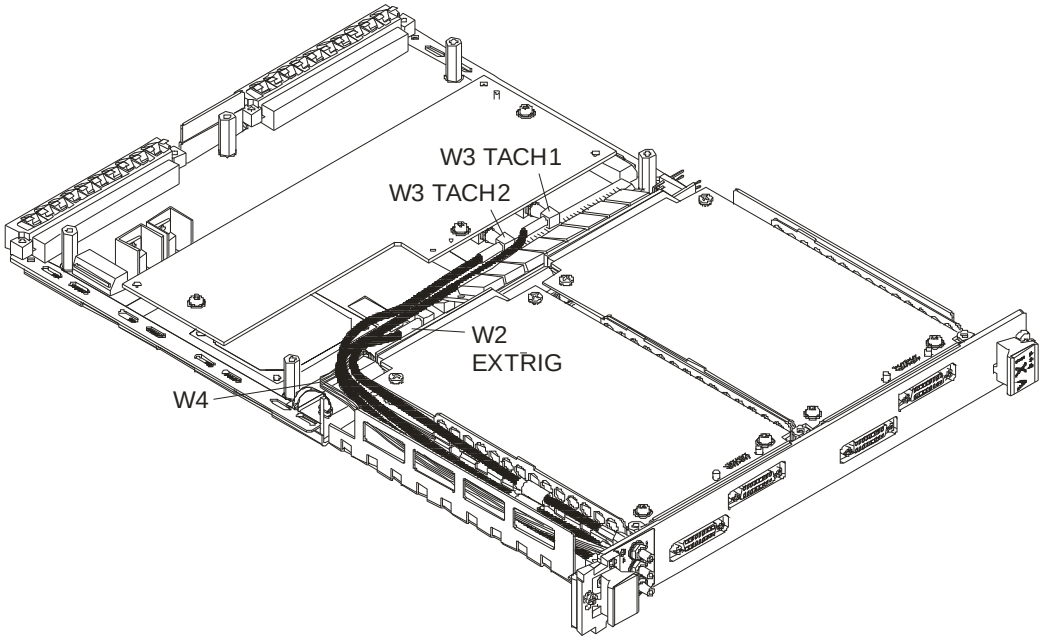
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2	52-0459-000	4	VT1432B PC ASSY-INPUT	03LB1	52-0459-000
A2	52-0560-000	4	VT1435 PC ASSY-INPUT	03LB1	52-0560-000
A4	E1432-66504	1	PC ASSY-LED	66049	E1432-66504
A10	E1433-66910	1	PC ASSY-MAIN OPT -UGV	03LB1	E1433-66510
A11	E1433-66911	1	PC ASSY-MAIN	03LB1	E1433-66511
A22	1818-5622	1	ICM DRAM, SIMM, 8x32	N121	MT16D832M-6
A24	1818-5624	1	ICM DRAM, SIMM, 1x32	N90	HYM532100AM-70
A41	E1432-66541	1	PC ASSY-OPT -1D4	03LB1	E1432-66541
MP001	41-0403-000	1	SHTF CVR-BTTM ALSK	03LB1	41-0403-000
MP002	41-0402-000	1	SHTF CVR-TOP	03LB1	41-0402-000
MP003	8160-0862	2	GSKT RFI STRIP FNGRS	N109	0786-318
MP004	0515-2033	5	SCR-MCH M3.0 10MMLG	N091	0515-2033
MP005	0515-2028	4	SCR-MCH M2.5 6MMLG	N091	0515-2028
MP006	E1432-44101	1	GSKT THERMAL CONDUCTOR	N046	E1432-44101
MP007	E1485-40601	1	GSKT-RFT, TOP CVR ADH SHT	77824	5774-194W-0
MP008	0515-0372	3	SCR-MCH M3.0 8MMLG	93907	0515-0372
MP009	8160-0634	4	STMP SHLD-RFI GRND	N109	8160-0634
MP010	8160-0686	1	STMP FNGRS-RFI STRP BECU	N109	786-185
MP011	8160-0683	1	STMP STRP-SPNG FLTR GRD	N109	0097-551-17-X
MP012	8160-0869	6	GSKT RFI, 2MM X 4MM	77824	E8119T00090
MP013	0515-0368	2	SCR-MCH M2.5 X 0.45	N091	0515-0368
MP014	0380-4042	5	STDF-HXMF M3.0 16.7MMLG	05791	SS5172-16.7-01
MP015	0380-4041	3	STDF-HXMF M3.0	05791	SS5172-15.0-01
MP016	0515-2383	2/4	SCR-MCH M3.0 12MMLG	N091	0515-2383

Cables: without Option AYF or 1D4



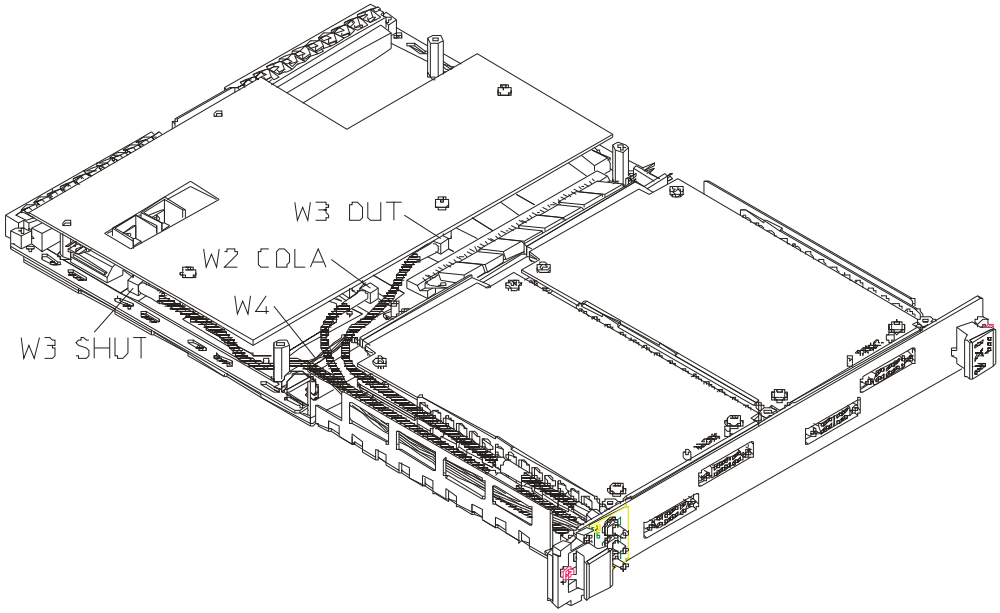
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
W1	8120-6767	1	CBL-ASM CXL, W/FE	N116	224743
W2	8120-6765	2	CBL-ASM CXL, W/FE	N116	224741
W4	8120-6762	1	RIBBON CABLE	N118	8120-6762

Cables: with Option AYF



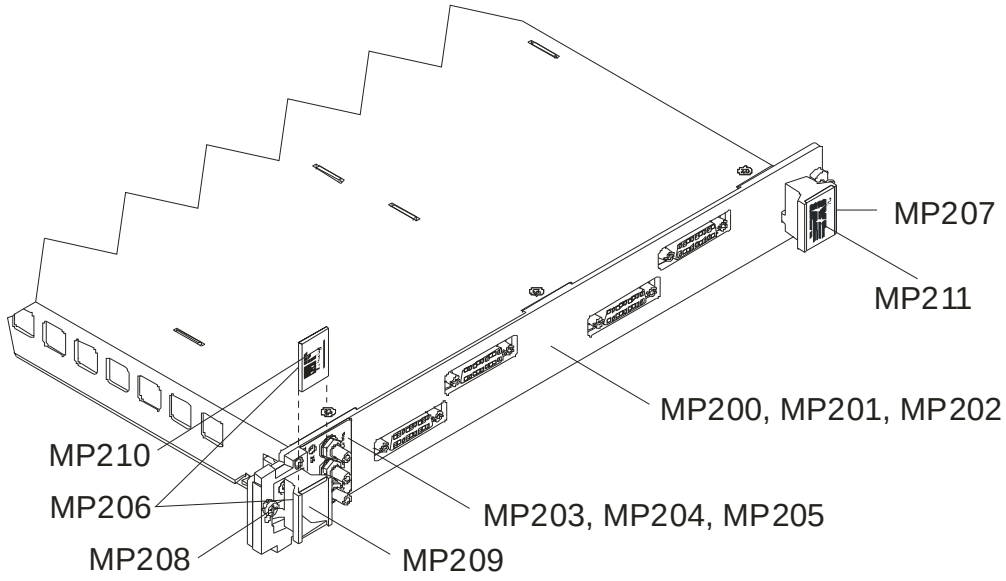
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
W2	8120-6765	2	CBL-ASM CXL, W/FE	N116	224741
W3	8120-6766	2	CBL-ASM CXL, 03LB1	N116	8120-6766
W4	8120-6762	1	RIBBON CABLE	N118	8120-6762

Cables: with Option 1D4



Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
W2	8120-6765	2	CBL-ASM CXL, W/FE	N116	224741
W3	8120-6766	2	CBL-ASM CXL, 03LB1	N116	8120-6766
W4	8120-6762	1	RIBBON CABLE	N118	8120-6762

Front Panel 1432B



Ref Res	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
MP200	41-0442-001	1	VT1432B 16 CH PNL-FRT, STNDRD	03LB1	41-0442-001
MP201	41-0442-000	1	VT1432B 8 CH PNL-FRT, OPT -1DE	03LB1	41-0442-000
MP202	41-0442-002	1	VT1432B 4 CH PNL-FRT, OPT -1DD	03LB1	41-0442-002
MP203	E1432-44301	1	LBL-FRT PNL SMB'S, STD	0PL50	E1432-44301
MP204	E1432-44302	1	LBL-FRT PNL SMB'S, OPT -1D4	03LB1	E1432-44302
MP205	E1432-44303	1	LBL-FRT PNL SMB'S, OPT -AYF	03LB1	E1432-44303
MP206	E1400-84106	1	MOLD KIT-TOP EXTR HNDL	N144	20897-255
MP207	E1400-84105	1	MOLD KIT-BTTM EXTR HNDL	N144	20897-254
MP208	0515-1968	2	SCR-MCH M2.5 6MMLG	03LB1	0515-1968
MP209	0515-1375	2	SCR-MCH M2.5 6MMLG	93907	0515-1375
MP210	43-0016-003	1	LABEL, VXI EXT, VXI TECH, LOGO	03LB1	43-0016-003
MP211	43-0016-002	1	LABEL, VXI EXT, VXIBUS	03LB1	43-0016-002

Front Panel VT1435/36 Common Components

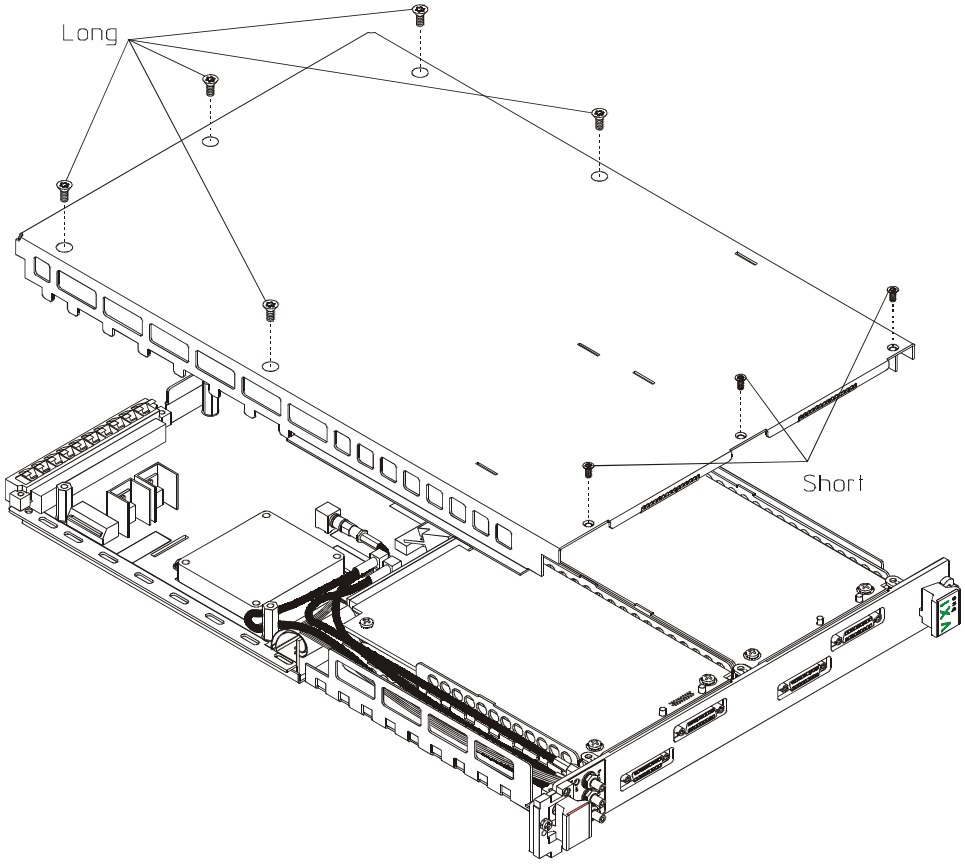
Ref Res	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
MP206	E1400-84106	1	MOLD KIT-TOP EXTR HNDL	N144	20897-255
MP207	E1400-84105	1	MOLD KIT-BTTM EXTR HNDL	N144	20897-254
MP208	0515-1968	2	SCR-MCH M2.5 6MMLG	03LB1	0515-1968
MP209	0515-1375	2	SCR-MCH M2.5 6MMLG	93907	0515-1375
MP210	43-0016-003	1	LABEL, VXI EXT, VXI TECH, LOGO	03LB1	43-0016-003
MP211	43-0016-002	1	LABEL, VXI EXT, VXIBUS	03LB1	43-0016-002

Front Panel VT1435 and VT1436

Ref Res	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
MP200	41-0443-000	1	VT1435 8 CH PNL-FRT, STNDRD	03LB1	41-0443-000
W/MP200	43-0158-000	1	VT1435 PNL-OVRLY, STNDRD	03LB1	41-0158-000
or					
W/MP200	43-0158-002	1	VT1435 PNL-OVRLY, TACH	03LB1	41-0442-002
or					
W/MP200	43-0158-004	1	VT1435 PNL-OVRLY, SOURCE	03LB1	41-0442-004
MP201	41-0443-001	1	VT1436 16 CH PNL-FRT, STNDRD	03LB1	41-0443-001
W/MP201	43-0158-001	1	VT1436 PNL-OVRLY, STNDRD	03LB1	41-0158-001
or					
W/MP201	43-0158-003	1	VT1436 PNL-OVRLY, TACH	03LB1	41-0442-003
or					
W/MP201	43-0158-005	1	VT1436 PNL-OVRLY, SOURCE	03LB1	41-0442-005
MP202	41-0443-002	1	VT1435-1DD 4 CH PNL-FRT, STNDRD	03LB1	41-0443-002
W/MP202	43-0158-006	1	VT1435-1DD PNL-OVRLY, STNDRD	03LB1	43-0158-006
or					
W/MP202	43-0158-007	1	VT1435-1DD PNL-OVRLY, SOURCE	03LB1	43-0158-007
or					
W/MP202	43-0158-008	1	VT1435-1DD PNL-OVRLY, TACH	03LB1	43-0158-008

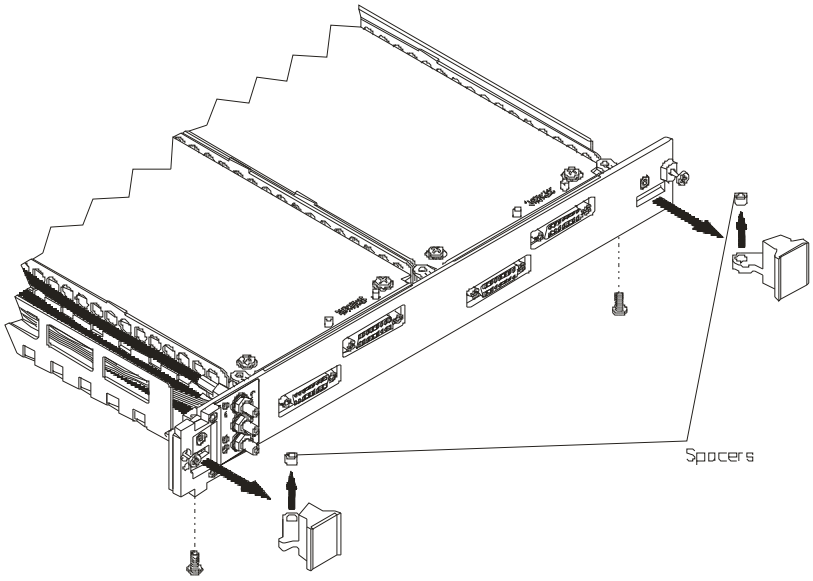
TO REMOVE THE TOP COVER

1. Remove the five long screws using a T-10 Torx driver and remove the three short screws using a T-8 Torx driver. Lift cover off.

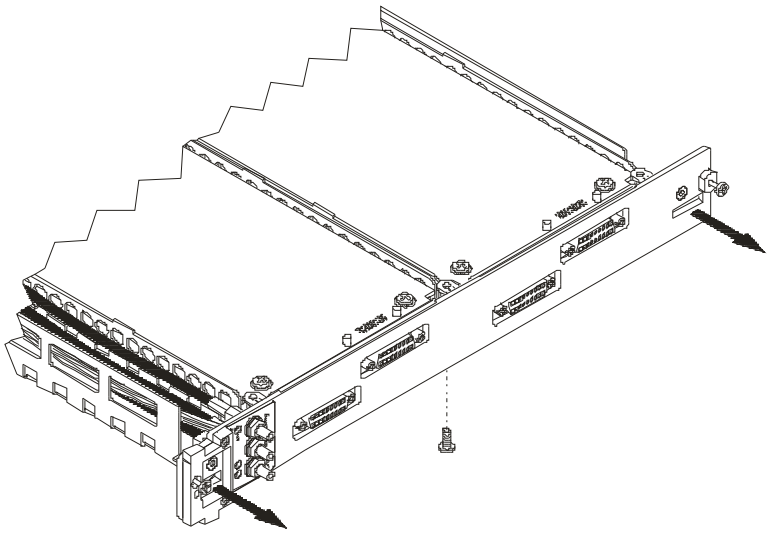


TO REMOVE THE FRONT PANEL

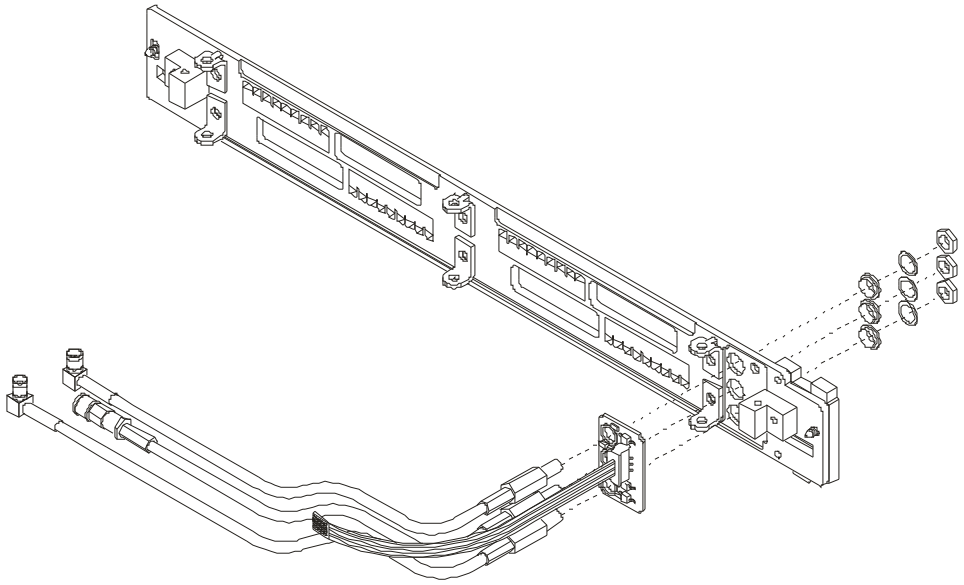
1. Remove top cover (see *To Remove the Top Cover*). Gently disconnect cables from the printed circuit assemblies. Using a T-8 Torx driver, remove the two screws that attach the handles to the assembly. Pull out the handles making sure not to lose the two spacers.



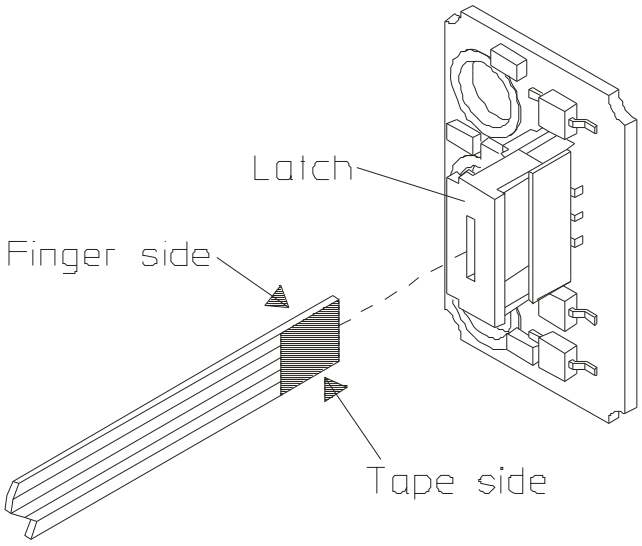
2. Using a T-8 Torx driver, remove the screw that attaches the front panel to the bottom cover. Gently pull the front panel off.



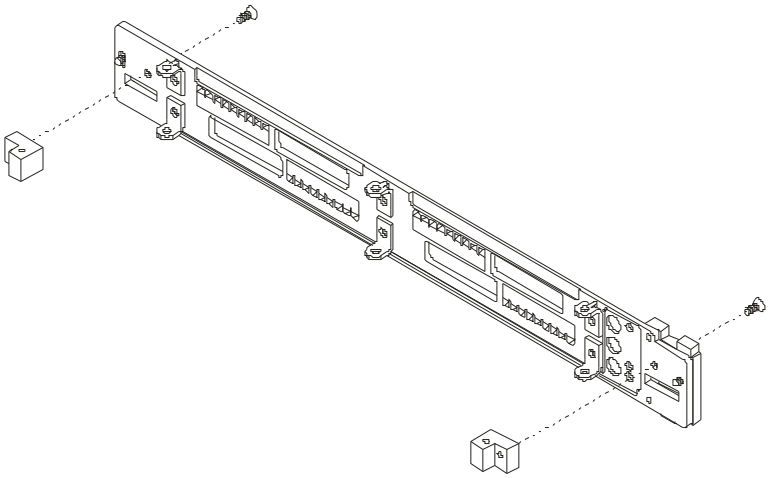
3. Remove the nuts that fasten the cables and assembly to the front panel. Using a 1/4-inch nut driver.



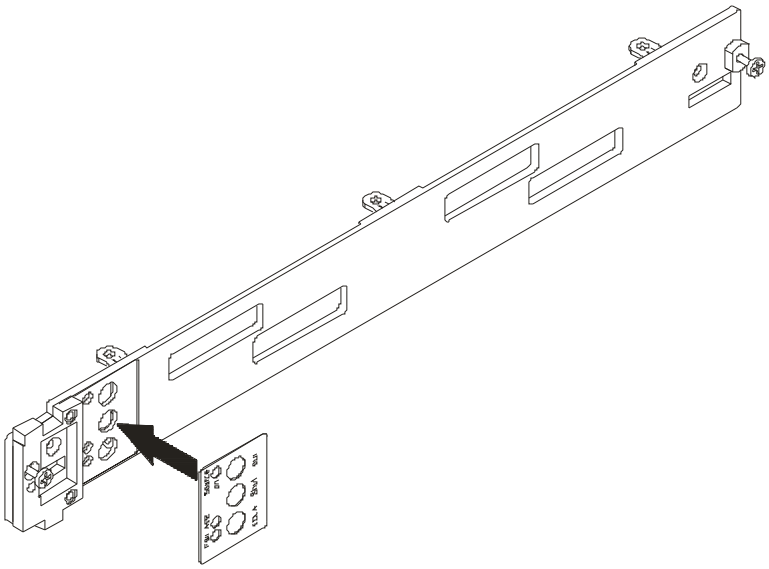
4. Remove ribbon cable from the A4 assembly, by pulling back the latch on the connector and removing cable. Be sure to note the orientation of the cable.



5. To replace the front panel with another that does not have its own side brackets, remove the brackets from the old front panel using a T-8 Torx driver. Be sure to note the positioning of the brackets, alignment is critical.



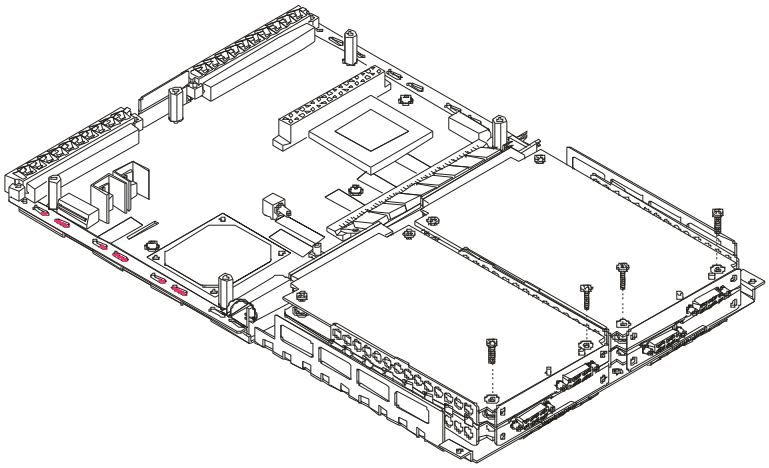
6. To replace the front panel with another that does not have the label already attached, remove the tape backing and place it on the front panel as shown. (VT1432B only)



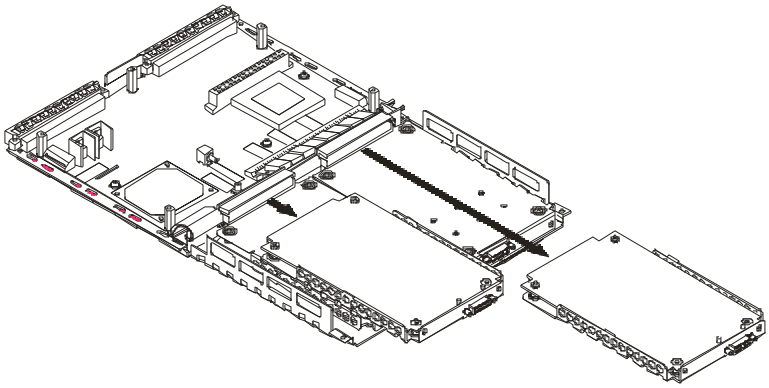
TO REMOVE THE INPUT ASSEMBLIES

1. Remove top cover (see To Remove the Top Cover). Remove the front panel (see steps 1 and 2 in To Remove the Front Panel). Note that the following steps are showing illustrations of a VT1432B with a standard configuration (four input assemblies). If the VT1432B has option 1DE (two input assemblies), the following steps will be the same except the length and quantity of screws.

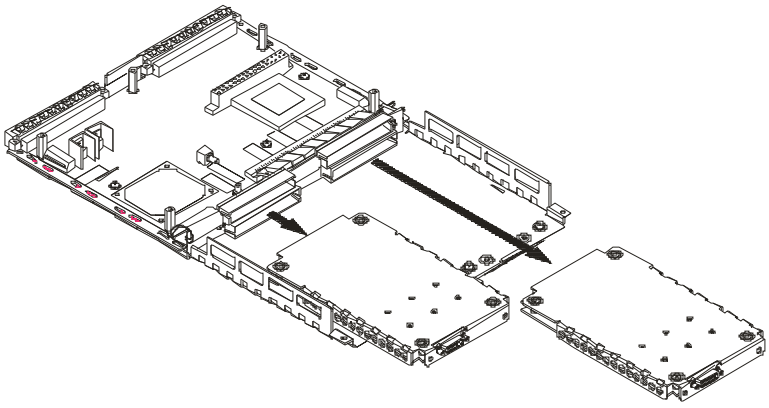
2. Using a T-10 Torx driver, remove the four screws that attach the assemblies to the bottom cover.



3. Remove the top two assemblies by gently pulling them forward, releasing them from the connectors.



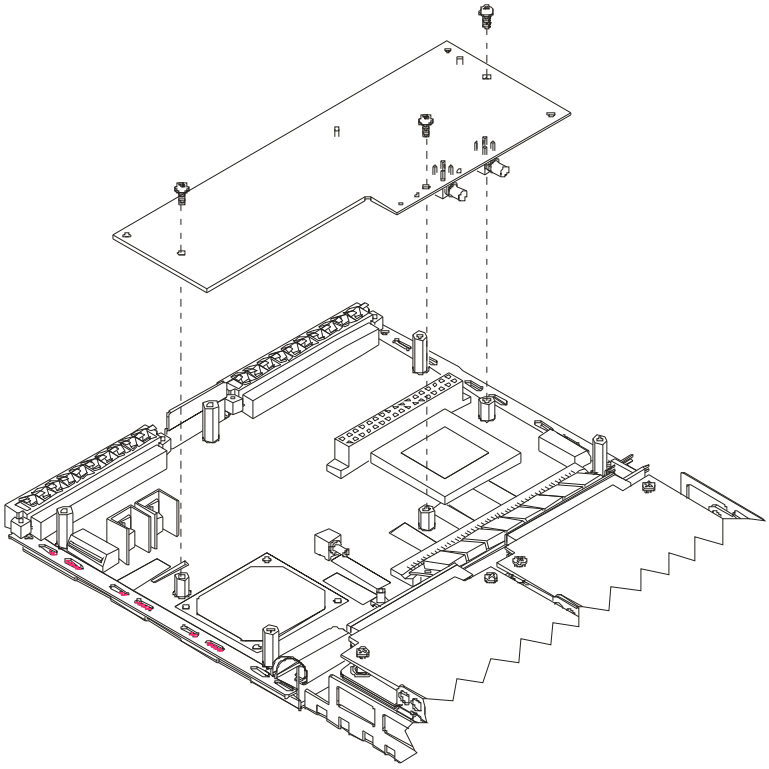
4. Remove the remaining input assemblies.



TO REMOVE THE OPTION AYF ASSEMBLY

1. Remove the top cover (see *To Remove the Top Cover*). Disconnect the three cables leading to the A41 assembly and move cables aside.

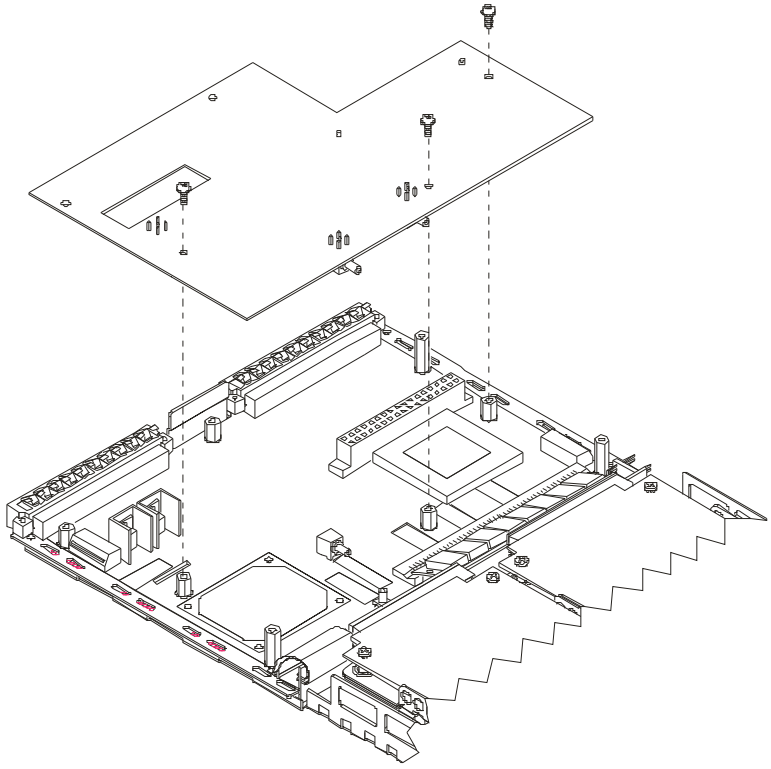
2. Using a T-10 Torx driver, remove the three screws that attach the assembly to the module's motherboard and lift the assembly off.



TO REMOVE THE OPTION 1D4 ASSEMBLY

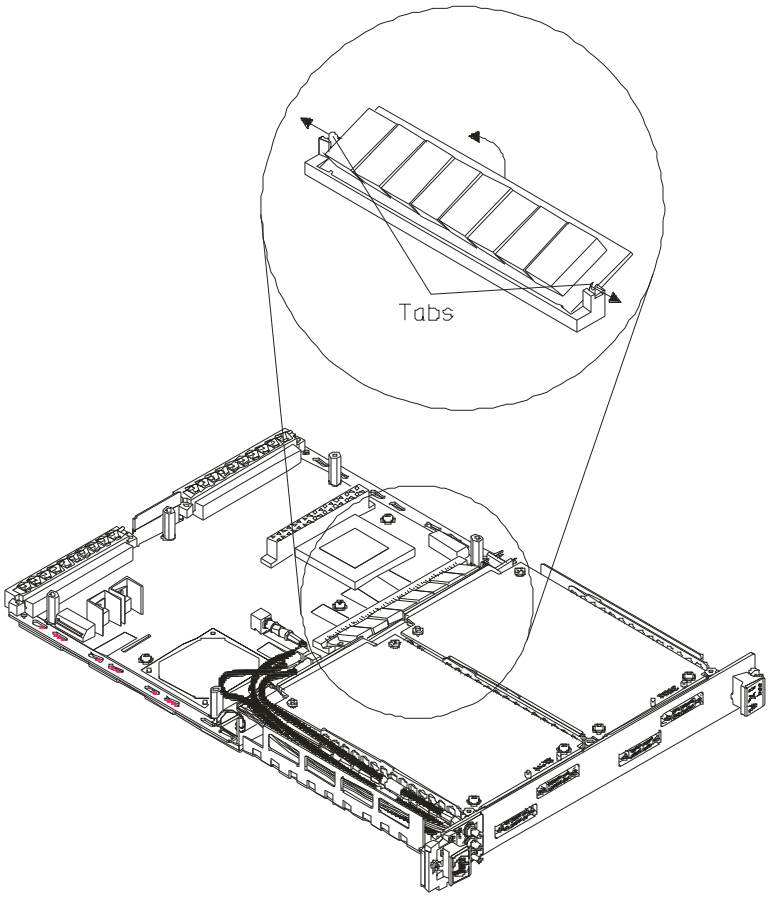
1. Remove the top cover (see *To Remove the Top Cover*). Disconnect the three cables leading to the A41 assembly and move cables aside.

2. Using a T-10 Torx driver, remove the three screws that attach the assembly to the module's motherboard and lift the assembly off.



TO REMOVE THE A22/A24 ASSEMBLY

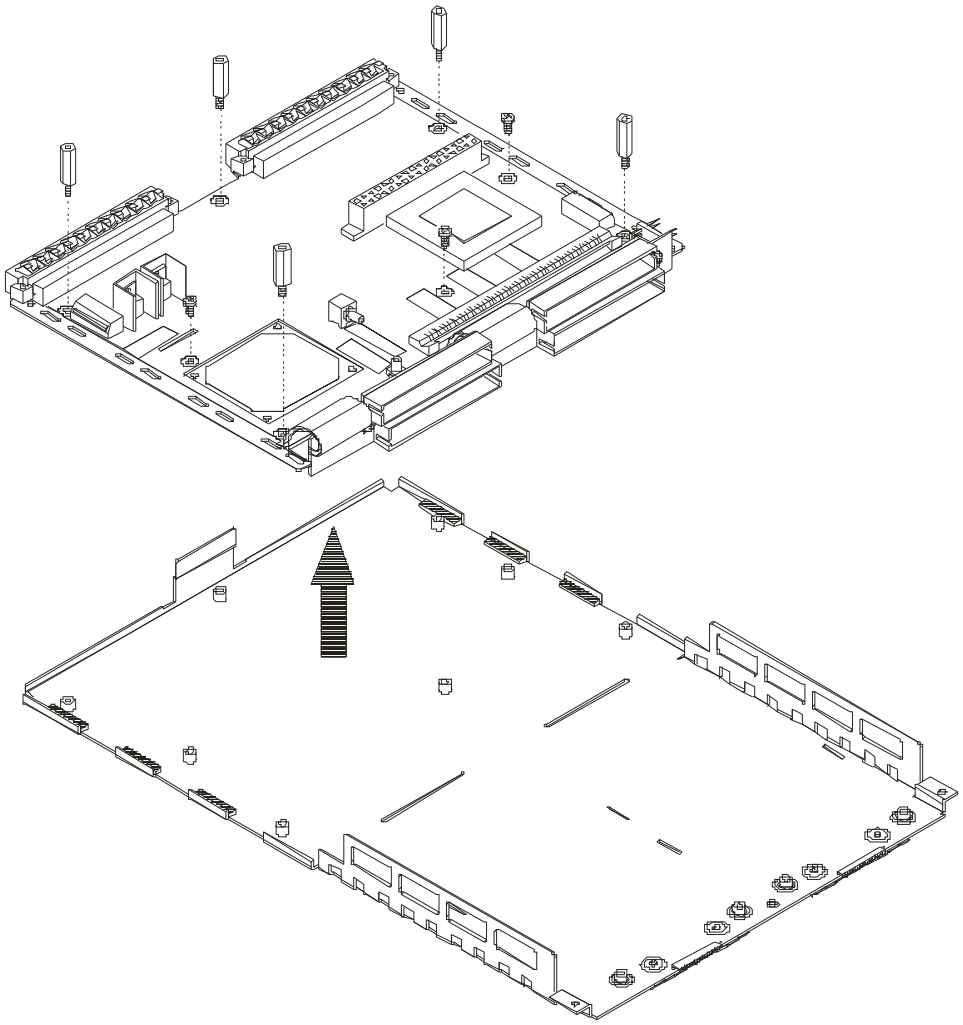
1. Remove the top cover (see *To Remove the Top Cover*). Gently push the silver tabs outward and tilt the A22/A24 assembly forward releasing it from the connector.



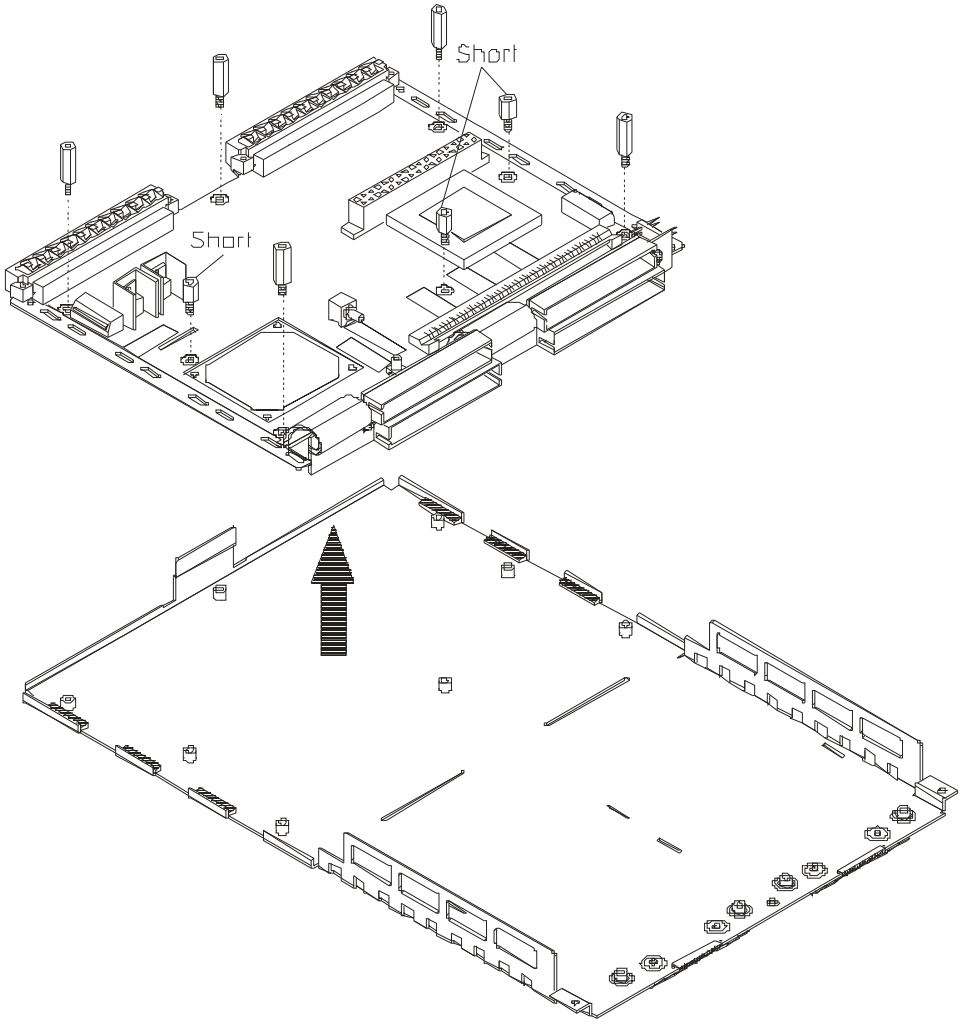
TO REMOVE THE A10/A11 ASSEMBLY

1. Remove top cover and input assemblies. See (To Remove the Top Cover and To Remove the Input Assemblies).

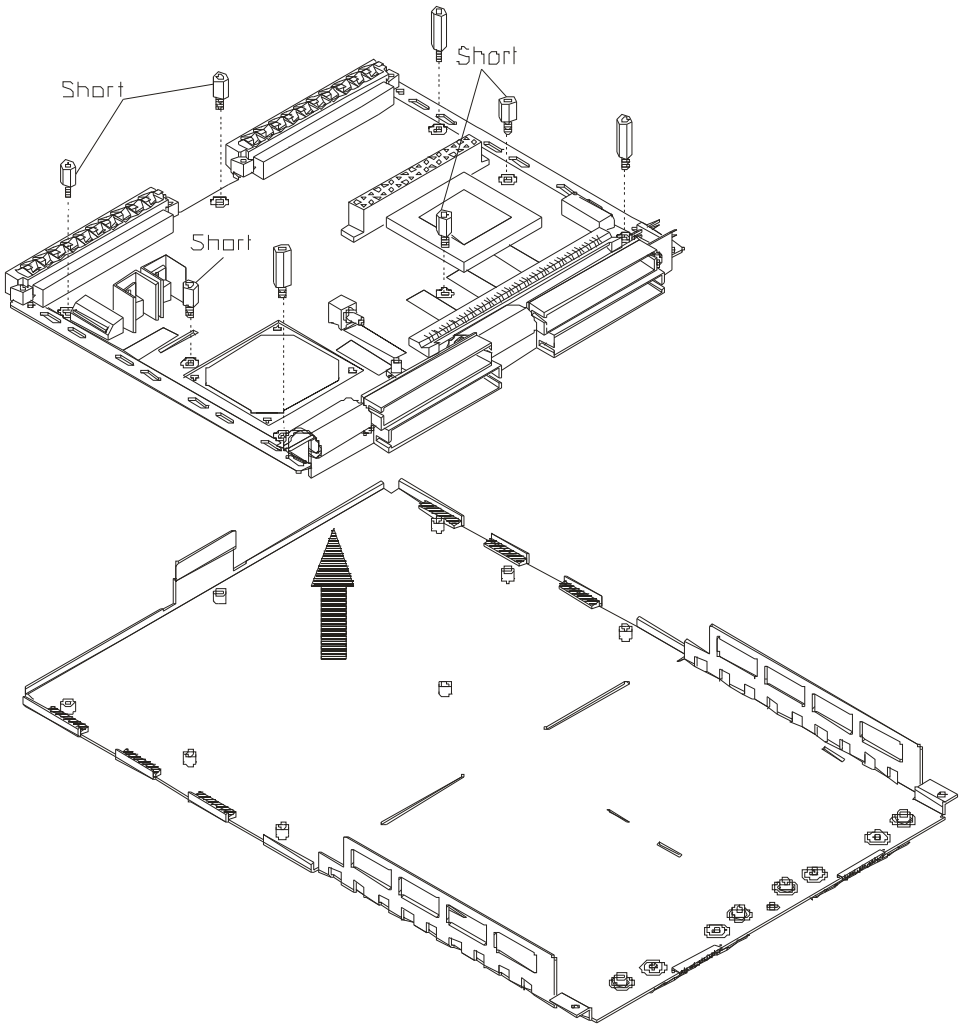
2. If the module does NOT have option AYF or option 1D4, do the following: Remove the five standoffs using a 1/4-inch nut driver and remove the three screws using a T-8 Torx driver. If option AYF is installed, proceed to step 0. If option 1D4 is installed, proceed to step 0.



3. If the module has option AYF, do the following: Remove the AYF option assembly see (*To Remove the Option AYF Assembly*). Remove the five long and the three short standoffs using a 1/4-inch nut driver.



4. If the module has option 1D4, do the following: Remove the 1D4 option assembly (see *To Remove the Option 1D4 Assembly*). Remove the three long and the five short standoffs using a 1/4-inch nut driver.



APPENDIX A

REGISTER DEFINITIONS

THE VT1432B REGISTER DEFINITIONS

The VT1432B 8- and 16-channel 102.4 kSa/s digitizers plus DSP are register-based VXI devices. Unlike message-based devices that use higher-level programming using ASCII characters, register-based devices are programmed at a very low level using binary information. The greatest advantage of this is speed. Register-based devices communicate at the level of direct hardware manipulation and this can lead to much greater system throughput.

Users do not need to access the registers in order to use the VT1432B. The VT1432B's functions can be more easily accessed using the VT1432B Host Interface Library software. However, this section describing the registers is provided as supplemental information.

The A16 Registers

The following A16 registers are accessible at the base address defined by the device's logical address. The register at offsets 00_{16} to $0E_{16}$ are not accessible using longword (D32) accesses. The registers at offsets 10_{16} to $3E_{16}$ may be accessed by any of the D08 (EO), D16, or D32 modes. All of these registers are also accessible at the device A24 base address.

Address	Read	Write
$3E_{16}$	Parameter 7 Register	
$3C_{16}$		
$3A_{16}$	Parameter 6 Register	
38_{16}		
36_{16}	Parameter 5 Register	
34_{16}		
32_{16}	Parameter 4 Register	
30_{16}		
$2E_{16}$	Parameter 3 Register	
$2C_{16}$		
$2A_{16}$	Parameter 2 Register	
28_{16}		
26_{16}	Parameter 1 Register	
24_{16}		
22_{16}	Query Response Register	Command Register
20_{16}		
$1E_{16}$	FIFO Count	
$1C_{16}$		
$1A_{16}$	Send Data	Receive Data
18_{16}		
16_{16}	RAM 1	
14_{16}		
12_{16}	RAM 0	
10_{16}		
$0E_{16}$	IRQ Status Register	IRQ Reset Register
$0C_{16}$	IRQ Config Register	
$0A_{16}$	Page Map Register	
08_{16}	Port Control Register	
06_{16}	Offset Register	
04_{16}	Status Register	Control Register
02_{16}	Device Type	
00_{16}	ID Register	Logical Address Register

The A24 Registers

The following A24 registers are accessible at the base address defined by the device's offset Register. The registers at offsets 00_{16} to $0E_{16}$ are not accessible using longword (D32) accesses. The registers at offsets 10_{16} to $FFFFF_{16}$ may be accessed by any of the of the D08 (EO), D16, or D32 modes.

F FFFF$_{16}$ 8 0000$_{16}$	Movable DSP Bus Window
7 FFFF$_{16}$ 3 0000$_{16}$	Fixed DSP Bus Window
2 FFFF$_{16}$ 2 0000$_{16}$	Send/Receive Data Registers
1 FFFF$_{16}$ 0 004F$_{16}$	Fixed DSP Bus Window
0 003F$_{16}$ 0 0000$_{16}$	VXIbus A16 Registers

The A24 registers are defined as follows:

- VXIbus A16 Registers: These are the same registers accessed at the device's A16 base address.
- Fixed DSP Bus Window: Accesses to this region are mapped to the corresponding locations at the base of the internal DSP's memory map, also accessible through Page 0 of the moveable DSP bus window.
- Send/Receive Data Registers: Accesses to any address in this region will read/write the Send and Receive Data registers defined in the A16 register set. VME Bus D32 Block Transfers are supported for these addresses only.
- Movable DSP Bus Window: Accesses to this region are mapped (by the Page Map register) to different 512 kB regions of the internal DSP bus.

The VXI Bus Registers are defined as follows:

- ID Register: A read of this 16-bit register provides information about the device's configuration. Its value is always $CFFF_{16}$ as defined in the following table.

Bit	15-14	13-12	11-0
Contents	11 (Register Based Device)	00 (A16/A24)	111111111111 (ID)

- Logical Address Register: A write to this register changes the device's logical address according to the VXI bus Dynamic Configuration protocol. Its format is defined in the following table.

Bit	15-8	7-0
Contents	No effect	Logical Address

- Device Type Register: A read of this register provides information about the device's configuration. Its format is defined in the following table.

Bit	15-12	11-0
Contents	0011 (1 MB of A24)	Model Code (201_{16} for VT1432B)
Contents	0011 (1 MB of A24)	Model Code (205_{16} for VT1435/36)

- Status Register: A read of this register provides information about the device's status as defined in the following table.

Bit	15	14	13-12	11	10	9	8
Contents	A24 Active	MODID*	Unused	Block Ready	Data Ready	ST Done	Loaded

Bit	7	6	5	4	3	2	1	0
Contents	Done	Err*	Unused	HW OK	Ready	Passed	Q Resp Ready	Cmd Ready

A24 Active: A one (1) in this field indicates that the A24 registers can be accessed. It reflects the state of the Control register's A24 Enable bit.

MODID*: A one (1) in this field indicates that the device is not selected via the P2 MODID line. A zero (0) indicates that the device is selected by a high state on the P2 MODID line.

Unused: A read of these bits will always return zero (0).

Block Ready: A one (1) indicates that there is a block of data available to be read from the Send Data registers. A zero (0) indicates that less than a full block is available.

Data Ready: A one (1) indicates that there is at least one word (32 bits) of data available in the Send Data register. A zero (0) indicates that there is not valid data in the Send Data register.

ST Done: A one (1) indicates that the internal DSP has competed and passed its self-test.

Loaded: A one (1) indicates that the internal DSP has successfully booted and has loaded a valid model code.

Done: A zero (0) indicates that the on-card microprocessor has not finished processing the last command and the Err* bit is not valid. This bit is set and cleared by the DSP.

Err*: A zero (0) indicates that an error has occurred in communicating with the DSP (for example: invalid parameters). This bit is set and cleared by the DSP.

Ready: The meaning of this depends on the state of the Passed bit. While Passed is false, a one (1) indicates that the device is in the Config Reg Init state and the Model Code bits of the Device Type register are not valid, while a zero (0) indicates that the device is in either the self-test or failed state. When Passed is true, a one (1) indicates that the DSP has finished its initialization and is ready for normal operation, while a zero (0) indicates that the device is in the passed state.

Passed: A zero (0) indicates that the device is in either the Hard Reset, Soft Reset, Config Reg Init, Failed, or Init Failed state. A one (1) indicates that the device is in the passed state.

HW OK: A one (1) indicates that all the on-card FPGAs have successfully be initialized.

Q Resp Ready (Query Response Ready): A one (1) indicates that the Query Response Register is loaded and ready to be read. It is set by the DSP and cleared in hardware by a write to the Command Register.

Cmd Ready: A one (1) indicates that the command register and parameter register are available for writing. It is set by the DSP microprocessor and cleared in hardware by a write to the Command Register. When this bit is zero (0), it additionally indicates that the Done bit is not valid.

- Control Register: A write to this register causes specific actions to be executed by the device. The actions are described in the following table.

Bit	15	14-2	1	0
Contents	A24/A32 Enable	Unused	Sysfail Inhibit	Reset

A24/A32 Enable: A one (1) in this field enables access to the device's A24 VME Bus registers. A zero (0) disables such access.

Sysfail Inhibit: A one (1) disables the device from driving the SYSFAIL* line.

Reset: A one (1) forces the device into a reset state.

- Offset Register: This read/write register defines the base address of the device's A24 registers. The four most significant bits of the Offset register are the values of the four most significant bits of the device's A24 register addresses. The 12 least significant bits of the Offset register are always zero (0). Thus, the Offset register bits 15-12 map the VME Bus address lines A23-A20 for A24 register accesses. A read of the Offset register always returns the address offset most recently written to the Offset register.
- Port Control Register: This register is used to override the Local Bus control of the device. (This applies to VT1432B modules that are equipped to use Local Bus.) It has the following format:

Bit	15-2	1	0
Contents	Unused	LBus Pipe	LBus Enable

LBus Pipe: Writing a one (1) puts the Local Bus into pipeline mode, if the LBus Enable bit is also set. Writing a zero (0) allows the Local Bus to operate in some other mode.

LBus Enable: Writing a one (1) enables the Local Bus interface. Writing a zero (0) disables the local bus interface. RESET VALUE: 0

- Page Map Register: This read/write register defines the internal location of the movable window into the device's DSP bus. (This 512 kB window begins at 512 kB into the device's A24 registers.) The eight least significant bits of the Page Map register are the page number. These bits are mapped to the internal DSP bus address lines as follows:

Bit 0:	DSP A(17)
Bit 1:	DSP A(18)
Bit 2:	DSP A(19)
Bit 3:	DSP A(20)
Bit 4:	DSP A(21)
Bit 5:	DSP A(22)
Bit 6:	DSP A(30) and A(24)
Bit 7:	DSP A(31)

The eight most significant bits of the Page Map Register are always zero (0).

- IRQ Config Register: This register configures the first VME Bus interrupt source. It provides for selection of the VME Bus IRQ level used and a bit mask. It has the following format:

Bit	15-8	7-4	3	2-0
Contents	Mask	Unused	IRQ Enabled	IRQ Line

Mask: This is a bit mask used to enable up to eight interrupt causes. A bit value of zero (0) disables the corresponding interrupt source. RESET VALUE: 0

IRQ Enable: A one (1) in this bit enables the generation of IRQ's. A zero (0) resets each of the eight interrupt causes and status bits. RESET VALUE: 0

IRQ Line: This field selects which VME Bus IRQ line is driven by this device. A value of zero (0) disconnects the interrupt source. RESET VALUE: 0

- IRQ Status Register: This read-only register indicates the reason for asserting the VME Bus interrupt. The format of the data is identical to that of the Status/ID word returned by an interrupt acknowledge (IACK) cycle. It differs from the IACK cycle in that the IACK cycle will clear the status bits and cause the de-assertion of the IRQ line. The register has the following format:

Bit	15-8	7-0
Contents	Status	Logical Address

Status: Each of these bits indicates the status of a cause of interrupt. A one (1) in a bit position indicates that the corresponding source is actively requesting and interrupt.

Logical Address: This is the device's current logical address.

- IRQ Reset Register: This register is used to reset the interrupt function. It has the following format:

Bit	15-8	7-0
Contents	Reset Bits	Unused

Reset Bits: Writing a one (1) to any of these bits will clear the corresponding bit in the IRQ status register. This will not disable subsequent interrupt generation. Clearing all of the IRQ status bits will cause the de-assertion of the IRQ line. Writing a zero (0) has no effect.

- Ram 0-1: These are 32-bit general-purpose RAM locations which are also accessible to the on-board DSP. See the following section regarding D16/D08 access of 32-bit registers.
- Send Data Register: Reading this register gets the next available word from the measurement data FIFO. The measurement data FIFO is a 32-bit device. See the following section regarding D16/D08 access of 32-bit registers.
- Receive Data Register: Writing to this register puts a word into the source data FIFO. The source data FIFO is a 32-bit device. See the following section regarding D16/D08 access of 32-bit registers.
- Count Register: The Count register contains an unsigned 16-bit integer which is the number of 16-bit words of data which are currently available from the Send Data register or which the Receive Data register is currently ready to accept. While a device is generating or accepting data, the Count register may indicate fewer than the actual number of words available.
- Query Response/Command Register: This register is used to send commands to and receive responses from the device. It is implemented as a 32-bit RAM location. Writing the least significant byte (highest address) clears the Command/Parameter Ready and Query Response Ready bits in the status register and interrupts the on-board DSP. See the following section regarding D16/D08 access of 32-bit registers and the communication protocol.
- Parameter 1-7 Registers: These are 32-bit RAM locations used to pass parameters along with commands to the device or query responses from the device. See the following section regarding D16/D08 access of 32-bit registers and the communication protocol.

32-bit Registers

Several of the A16 registers (and all other 24-bit registers) are implemented as 32-bit-only resources. These are accessible using VME Bus D16 and D08 (EO) accesses. However, certain restrictions apply. The affected A16 registers are:

- RAM 0-1
- Send Data
- Receive Data
- Query Response Command

- Parameter 1-7
- Reading 32-bit Registers

Reading 32-bit Registers

When reading a 32-bit register using 8- or 16-bit modes, a simple caching mechanism is used. On any read including the most significant byte (lowest address), the 32-bit register is read and all 32 bits are latched into the read cache. A read not including the most significant byte fetches data from the read cache without re-reading the register. This insures that the data will be unchanged by any intervening write by the DSP (which would result in garbled data).

This mechanism also introduces a hazard. Reads of less significant bytes get data from the 32-bit register last read by a most-significant-byte read. In other words, the least significant byte cannot be read first or by itself. Thus, there are two important rules:

1) Always read all 32 bits of a 32-bit register.
2) Always read the most significant part first.

Writing 32-bit Registers

When writing to a 32-bit register using 8- or 16-bit modes, a simple caching scheme is also employed. On any write not including the least significant byte (highest address), the data is latched into the write cache. A write to the least significant byte causes the cached data to be written to the 32-bit register (in parallel with the current data for the least significant bytes(s)).

This mechanism has its own hazards. Writes to the least significant byte will always include the most recently cashed data, whether intended for that register or not. Lone writes to the most significant part of a 32-bit register will be lost if not followed by a write to the least significant part of the same register. Thus, there are two important rules:

1) Always write all 32 bits of a 32-bit register.
2) Always write the least significant part last.

Command/Response Protocol

The Command/Response protocol uses the following resources:

- Command/Query Response register implemented as a general purpose RAM
- Three parameter registers implemented as a general purpose RAM
- Additional A24 accessible RAM contiguous with the parameter registers
- The Command Ready, Query Response Ready, Err*, and Done bits of the Status register.

The RAM registers are the communications media, while the Status register bits provide synchronization. In general, a controller sends a command to the DSP by first writing any parameters to the parameter registers and the following RAM location. It then writes the command to the command register, which clears the Command/Parameter Ready bit and interrupts the DSP. At this point, the DSP has exclusive access to the RAM registers. The controller may not access that RAM again until the Command/Parameter Ready bit is true.

When interrupted, the DSP reads the command and its parameters, writes any response data back to the Query Response Register and any other data to the parameter registers and the following RAM and set the Command/Parameter Ready bit true.

The Query Response Ready bit is used to indicate that the DSP has written query data to the RAM registers. It is set by the software and cleared by a write of the Command Register.

The Done bit is set by DSP software when it finishes execution of a command or a command sequence. This may be long after it has set the Command/Parameter Ready bit. The DSP software clears the Done bit immediately on receipt of a new command, before it sets the Command/Parameter Ready bit.

The Err* bit is asserted (to 0) by the DSP software to indicate an error in the decoding or execution of a command. It is asserted (to 1) if the command was executed with no error. This bit must be valid before Done is set at the end of a command.

In order to avoid contention and/or invalid data reads, there are certain rules that must be observed:

1) A controller must not write to any of the RAM registers when Command/Parameter Ready is false.
2) The DSP must not write to any of the RAM registers when either Command/Parameter Ready or Query Response Ready is true.
3) A controller must not read any of the RAM registers when Query Response Ready is false.
4) The DSP must not read any of the RAM registers when Command/Parameter Ready is true.
5) When writing a command together with parameter, a controller must always write to the Command Register last.
6) When executing a command that requires it to return response data, the DSP must set the Query Response Ready bit no later than the Command/Parameter Ready bit.
7) The DSP must not clear the Done bit while Command/Parameter Ready is true.
8) The DSP must not change the Err* bit while Done is true.
9) A controller must not regard the done bits a valid while Command/Parameter Ready is false.
10) A controller must not regard the Err* bit as valid while Done is false.

Controller Protocol Examples

There are three basic procedures used by a controller, Write Command, Read Response, and Wait for Done. These can be combined for more complex sequences.

Write Command

This is the procedure to send a command to the DSP.

1) Wait for Command/Parameter Ready true.
2) Write any parameters to the Parameter registers and RAM.
3) Write the command to the Command register.

Read Response

This is the procedure for reading a response to query command.

1) Wait for Query Response Ready true.
2) Read the data from the Query Response register and any additional data from the parameter registers and RAM.

Wait for Done

This is the procedure to wait for command completion and check for error.

1) Wait for Command/Parameter Ready true.
2) Wait for Done true.
3) If Err* = 0, handle error.

Complex Sequences

A robust procedure for sending a query and reading the response would look like this:

1) Send Command.
2) Wait for Done.
3) If no error then Read Response.

Multiple commands may be sent with a test for errors at the end of the sequence. This example sends three commands before checking for errors.

1) Send Command.
2) Send Command.
3) Send Command.
4) Wait for Done.

DSP Protocol

When a controller writes to the Command register, a DSP interrupt is generated. When responding to this interrupt, the DSP will follow this procedure.

1) Clear the Done bit.
2) Read and decode the command from the Command register.
3) Read any parameters from the Parameter registers and RAM.
4) If a response data is required:
   a. Write the data to the Query Response register, Parameter registers, and RAM.
   b. Set Query Response Ready true.
5) Set Command/Parameter Ready true.
6) Finish command execution.
7) If any errors are pending, set Err* = 0, else set Err* = 1.
8) Set Done true.

There are two additional requirements for the DSP:

1) Once it begins processing a command interrupt, the DSP must defer processing subsequent commands until it has finished.
2) The DSP software maintains an error(s) pending flag (and possibly and error queue) that is set by any command decoding or execution error and cleared by some other method such as an error query.

DSP Bus Registers

There are two 32-bit registers in the DSP bus address space. The VXI FPGA does not assert TA* when these registers are accessed.

$200A_{16}$	DSP Command Register
$200B_{16}$	Boot Register

Note that these registers appear multiple times in the memory map, since only the address lines A31-30, A17-13, A9-8, and A3-0 are used for decoding.

The A24 registers are defined as follows:

- Boot Register: This read/write register is used to configure the device after a device reset. It has the following format:

Bit	31-16	15	14	13	12	11-0
Contents	Unused	Spare	ST Done	Loaded	Ready	Model Code

Spare: This read/write bit has no pre-defined function.

ST Done: This bit should be written to a one (1) when the DSP successfully competes its self-test, within five seconds after SYSRESET* is de-asserted. Its initial value is zero (0).

Loaded: This bit should be written to a one (1) when (or immediately after) the DSP loads the model code, before competing its self-test. Its initial value is zero (0).

Ready: This bit is written to a one (1) to indicate that the device is ready for normal operation. Its initial value is zero (0).

Model Code: As soon as possible and within 25 ms after coming out of reset, when the DSP has valid code loaded, it should write the VXI model code to these bits. Their initial value is 0x0200.

- DSP Command Register: This register is used to assert VXI interrupts and toggle various status register bits. Many of the bits in this register are grouped into related Clock and Value pairs. This allows the bits to be modified independently with single register writes. In order to change an output value, the Clock bit must be written as a one (1), while the Value is written as the desired output value. Writing the Clock bit as a zero (0) will not change the output state. The current state is read from the Value bit.

The DSP Command register has the following format:

Bit	31-24	23	22	21	20	19	18	17	16
Contents	Unused	FIFO Enable Clock	FIFO Enable Value	FIFO In Clock	FIFO In Value	DONE Clock	DONE Value	ERRn Clock	ERRn Value

Bit	15	14	13	12	11	10	9-8	7-0
Contents	Q Resp Ready Clock	Q Resp Ready Value	Cmd Ready Clock	Cmd Ready Value	IRQ Enable Clock	IRQ Enable Value	Unused	IRQ7

APPENDIX B

GLOSSARY

A16 registers Address space using 16 address lines. The VXI definition gives each VXI module 64 bytes of A16 registers.

A24 registers Address space using 24 address lines. VXI modules can configure how much A24 address space they use.

Agilent VEE An Agilent program for graphical programming. See *VEE*.

arbitrary source A signal source capable of producing an arbitrary waveform according to the way it is programmed.

arbitration bus See DTB arbitration bus.

ASCII Abbreviation for *A*merican *S*tandard *C*ode for *I*nformation *I*nterchange, a standard format for data or commands.

backplane A set of lines that connects all the modules in a VXI system.

baseband A band in the frequency spectrum that begins at zero. By contrast, a zoomed band is centered on a specified center frequency.

block mode A mode of data collecting where the instrument stops taking data as soon as a block of data has been collected. Overlap block mode in the VT1432B and VT1433B can be configured to act exactly like block mode.

block size The number of sample points in a block of data.

breakout box Another name for the 8-channel input connector.

C-size One of several possible sizes for VXI modules. The VT1432B, VT1435, VT1436, and VT1433B are C-size modules.

Channel-dependent commands Commands that are channel dependent change a parameter for each channel independently.

COLA Abbreviation for *c*onstant *o*utput level *a*mplifier.

continuous mode A mode of data collecting used where the instrument collects data continuously and stops only if the FIFO overflows.

D32, D16, and D08 (EO) The VXI bus provides 32 data lines. Modules can use all 32 lines or 16 lines or 8 lines. For example, “D16 access” refers to data read across 16 lines.

daisy-chain A set of instruments or modules connected together in a line. Data and instructions enter each one before being buffered and passed out to the next module in line.

decimation filter	A digital filter that simultaneously decreases the bandwidth of the signal and decreases the sample rate. The digital filter provides alias protection and increases frequency resolution. For more information, see Spectrum & Network Measurements available through VXI Technology.
delta sigma	A method for converting an analog input to digital data. It involves using a difference of two voltages (delta) and a summation of signals (sigma) to improve accuracy.
digitizer	An instrument which converts analog signals into digital data suitable for digital signal processing.
DRAM	Abbreviation for *d*ynamic *r*andom *a*ccess *m*emory.
DSP	Abbreviation for *d*igital *s*ignal *p*rocessing (or processor).
DTB arbitration bus	The VT1432B does not use the arbitration bus. The arbitration bus is part of the VXI specification and is used by some modules to request bus control.
ECL	Abbreviation for emitter-collector logic, a standard for electrical signals.
Engineering Unit (EU)	A scale factor used to convert the output of a transducer (in volts) into another unit (for example: g's).
FFT	Abbreviation for *f*ast *F*ourier *t*ransform.
FIFO	Abbreviation for *f*irst-*i*n *f*irst-*o*ut. A buffer and controller used to transmit data. The FIFO in the VT1432B/VT1433B input is implemented using DRAM.
Free-run counter	A counter in which the bits always increment. When the free-run counter reaches all ones it resets to all zeros and continues counting.
f_s	Abbreviation for sample *f*requency or sample rate.
group ID	Any number of channels may be declared and uniquely identified by a groupID. A channel can be a member of more than one group.
holdoff time	A circuit that detects a trigger signal will not respond to another trigger until the hold-off time has passed. This prevents a ringing signal from be detected as multiple triggers.
IACK	Abbreviation for *i*nterrupt *ack*nowledge.
IEPE	Abbreviation for *i*ntegrated *e*lectronics *p*iezo*e*lectric.
IRQ	Abbreviation for *i*nterrupt *req*uest.
kSa/s	Abbreviation used for *k*ilo*sa*mples per *s*econd.
LED	Abbreviation for *l*ight *e*mitting *d*iode.
Local Bus	A high-speed port that is defined as a standard byte-wide ECL protocol which can transfer measurement data at up to 2.62 MSamples per second from left to right on the VXI backplane.
logical address	The VXI logical address identifies where each module is located in the memory map of the VXI system.

Message-based VXI device	Message-based devices communicate with the VXI bus using high-level ASCII commands. Programming is easier and more sophisticated, but communication is slower than with register-based devices. Message-based devices can also be programmed at the register level. The VT1432B, VT1435, VT1436, and VT1433B are register-based VXI devices.
module-dependent commands	Module-dependent commands change a parameter for all channels of the module; even when only one channel has been specified in the channel list.
MXI bus	A bus standard that can be used to connected multiple VXI mainframes.
overlap block mode	A mode of data collecting in used in the VT1432B and VT1433B. It is similar to block mode except that it allows additional arms and triggers to occur before an already-acquired block is sent to the host.
pipeline mode	A Local Bus mode in which data is sent through a module and on to the next one.
plug&play	See VXI*plug&play*
RAM	Abbreviation for *r*andom *a*ccess *m*emory.
register-based VXI device	Register-based devices communicate with the VXI bus by way of registers. They must be programmed with low-level binary commands but they can communicate faster than message-based devices. The VT1432B, VT1435, VT1436, and VT1433B are register-based VXI devices.
registers	Memory locations in the hardware of a VXI module that can be used to program the module at a low level.
RPM	Abbreviation for *r*evolutions *p*er *m*inute.
ROM	Abbreviation for *r*ead-*o*nly *m*emory.
sample rate	The rate at which the measurement data is sampled. For the VT1432B, the sample rate is 2.56 times the frequency span. Sample rate is abbreviated "f_s" (for "sample frequency").
SCA	Abbreviation for *s*ignal *c*onditioning *a*ssembly. Groups of four input channels are located on one SCA (Channels 1 through 4, channels 5 through 8, channels 9 through 12, and channels 13 through 16 are located on separate SCAs.)
Settling	When settling, the digital filter waits a designated number samples before outputting any data.
SFP	See *s*oft *f*ront *p*anel.
shared memory	Memory locations in both a VXI module and in a host or controller which are shared and can be used to transmit data between the host and module.
slot 0 commander	The module which occupies the left-most slot in a VXI mainframe. It supplies important signals for the rest of the system.
SMB	*S*ub-*m*iniature "*B*"; a type of connector.
Soft Front Panel	A VXI*plug&play* program which provides and easy-to-use interface for the VT1432B. It can be used in a Windows environment.
SRAM	Abbreviation for *s*tatic *r*andom *a*ccess *m*emory.

summer	A circuit that outputs the sum of two input signals.
sync/trigger line	A TTL line on the VXI backplane, used for synchronization or triggering signals.
SYSRESET*	SYStem RESET line, part of the VXI bus.
system module	The module with the lowest VXI logical address. It needs to be set to output the synchronization pulse for a multiple module group. All system sync pulses come from the system module.
tachometer	The tachometer produces a signal which is proportional to the rotation of a device. It can be programmed to produce one or more signals per revolution.
target	The 'target' of a library function is either a channel, a group or (rarely) a module, depending on the nature of the call. When the same library function may be called with either a channel or a group identifier, its 'target' is shown by a parameter named ID.
TEDS	Abbreviation for *t*ransducer *e*lectronic *d*ata *s*heet.
TTL	Abbreviation for transistor-transistor logic, a standard for electrical signals.
TTLTRG	TTL TRiGger lines, part of the VXI bus.
VEE	Abbreviation for virtual engineering environment, a program which facilitates the setup and programming of instruments by employing a graphic user interface.
VME Bus	An industry-standard bus on the VXI backplane for module control, setup and measurement data transfers. For measurement data transfers, the Local Bus offers higher transfer rates.
VXI	Abbreviation for VME extensions for instrumentation, a standard specification for instrument systems.
VXIplug&play	A set of standards which provides VXI users with a level of standardization across different vendors beyond what the VXI standard specifications spell out.
Zoom	In instruments that support zoom, one can select a frequency span around a specified center frequency in order to focus on a specific frequency band.

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